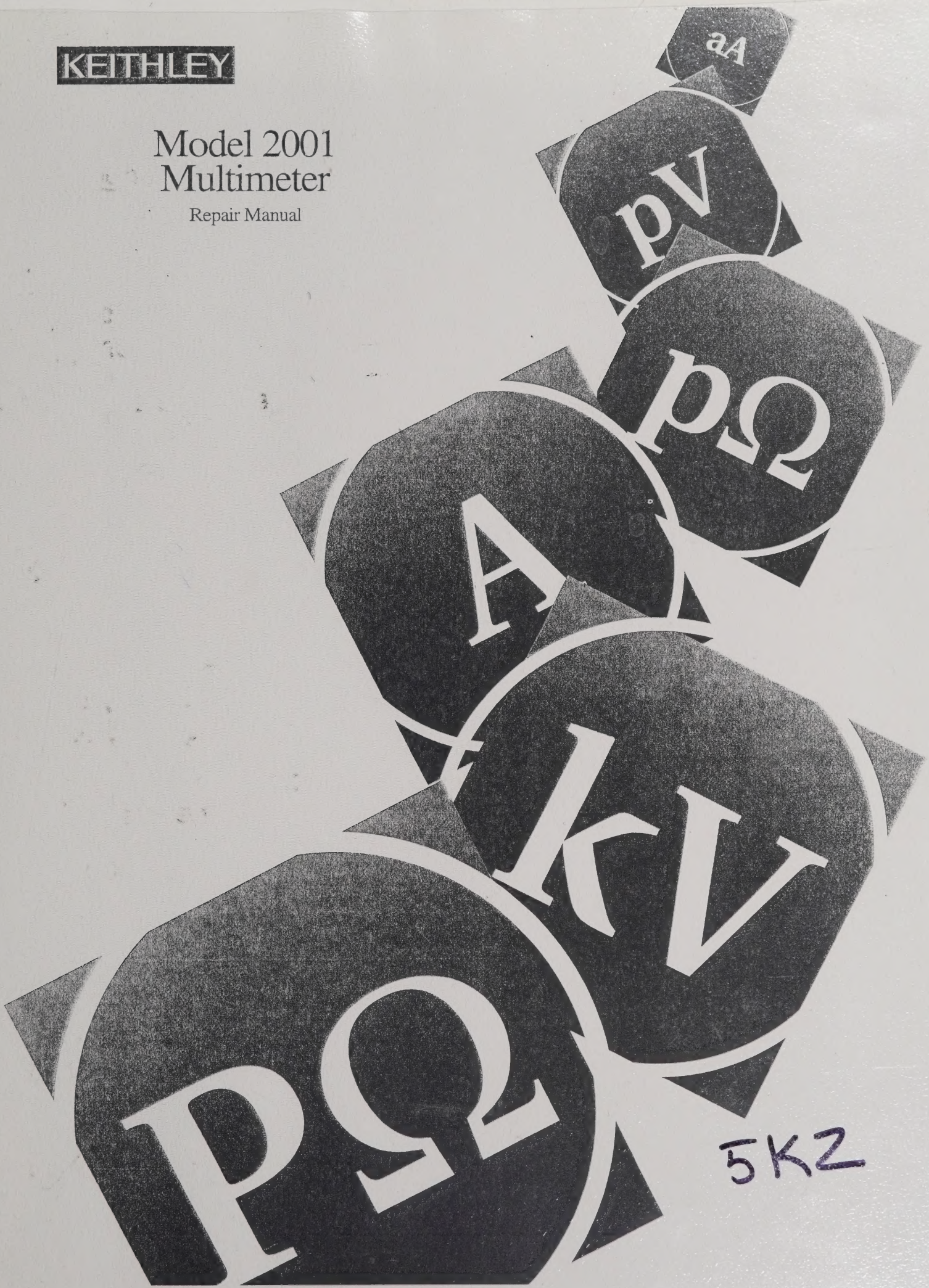
KEITHLEY

Model 2001 Multimeter

Repair Manual



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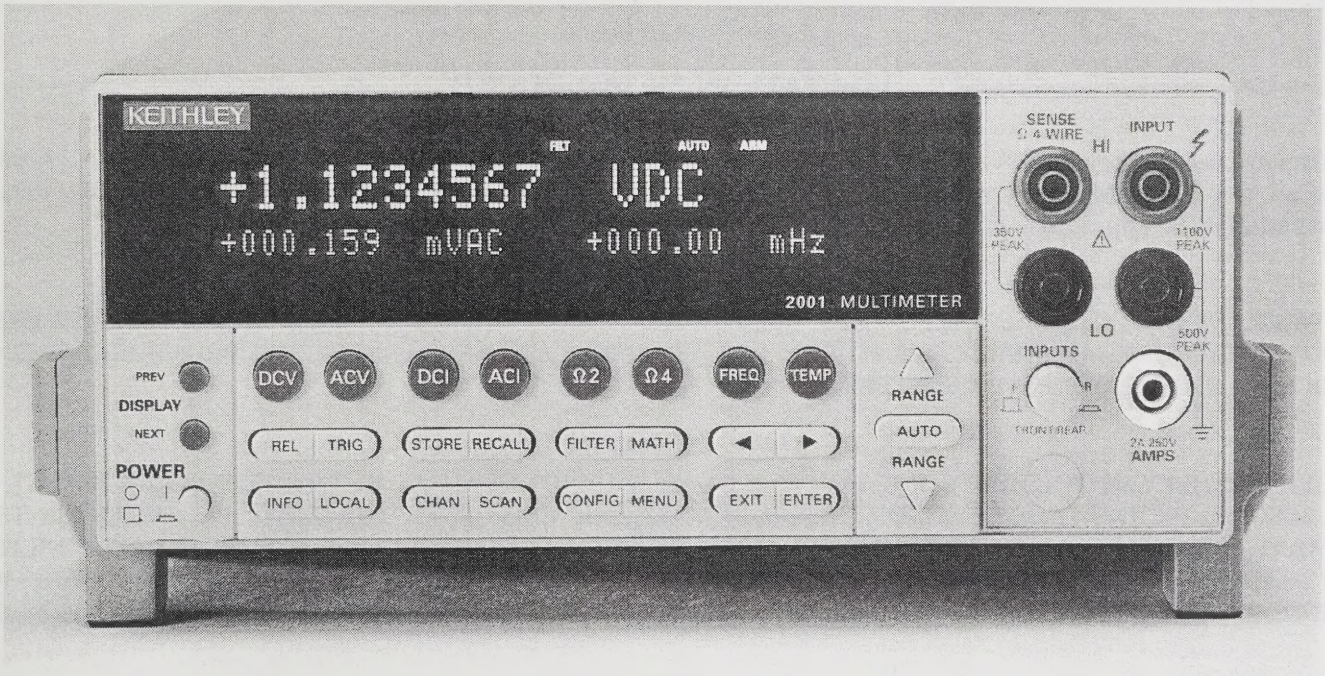
Model 2001 Multimeter

Repair Manual



Contains Servicing Information

KEITHLEY

WARRANTY

Keithley Instruments, Inc. warrants this product to be free from defects in material and workmanship for a period of 3 years from date of shipment.

Keithley Instruments, Inc. warrants the following items for 90 days from the date of shipment: probes, cables, rechargeable batteries, diskettes, and documentation.

During the warranty period, we will, at our option, either repair or replace any product that proves to be defective.

To exercise this warranty, write or call your local Keithley representative, or contact Keithley headquarters in Cleveland, Ohio. You will be given prompt assistance and return instructions. Send the product, transportation prepaid, to the indicated service facility. Repairs will be made and the product returned, transportation prepaid. Repaired or replaced products are warranted for the balance of the original warranty period, or at least 90 days.

LIMITATION OF WARRANTY

This warranty does not apply to defects resulting from product modification without Keithley's express written consent, or misuse of any product or part. This warranty also does not apply to fuses, software, non-rechargeable batteries, damage from battery leakage, or problems arising from normal wear or failure to follow instructions.

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Model 2001 Multimeter
Repair Manual

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Manual Print History

The print history shown below lists the printing dates of all Revisions and Addenda created for this manual. The Revision Level letter increases alphabetically as the manual undergoes subsequent updates. Addenda, which are released between Revisions, contain important change information that the user should incorporate immediately into the manual. Addenda are numbered sequentially. When a new Revision is created, all Addenda associated with the previous Revision of the manual are incorporated into the new Revision of the manual. Each new Revision includes a revised copy of this print history page.

Revision A (Document Number 2001-902-01) ..... April 1993
Revision B (Document Number 2001-902-01) ..... February 1996

Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read the operating information carefully before using the product.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture rear panel, or switching card.

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC main. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If a ⏚ screw is present on the test fixture, connect it to safety earth ground using #18 AWG or larger wire.

The ⚡ symbol on an instrument or accessory indicates that 1000V or more may be present on the terminals. Refer to the product manual for detailed operating information.

Instrumentation and accessories should not be connected to humans.

Maintenance should be performed by qualified service personnel. Before performing any maintenance, disconnect the line cord and all test cables.

Table of Contents

4 Replaceable Parts

List of Illustrations

1 Routine Maintenance

2 Troubleshooting

List of Tables

1 Routine Maintenance

2 Troubleshooting

4 Replaceable Parts

1 Routine Maintenance

1.1 Introduction

In general, the information in this section deals with routine type maintenance that can be performed by the operator. This information is arranged as follows:

1.2 Line fuse replacement — Explains how to replace a blown line power fuse.

1.3 Current fuse replacement — Explains how to replace a blown current fuse.

1.4 Fan filter cleaning — Explains how to remove and clean the filter element for the cooling fan.

1.5 Firmware updates — Recommends a course of action for firmware updates provided by Keithley.

1.2 Line fuse replacement

WARNING

Disconnect the line cord at the rear panel. Remove all test leads connected to the instrument (front and rear).

The power line fuse is accessible from the rear panel, just below the ac power receptacle (see Figure 1-1). Perform the following steps to replace the line fuse:

1. Insert a bladed screwdriver into the slot of the fuse carrier.
2. While pushing in, turn the screwdriver counterclockwise until the spring loaded fuse carrier releases from the fuse holder.
3. Pull out the fuse carrier and replace the fuse with the type specified in Table 1-1.

CAUTION

To prevent instrument damage, use only the fuse type specified in Table 1-1.

4. Re-install the fuse carrier.

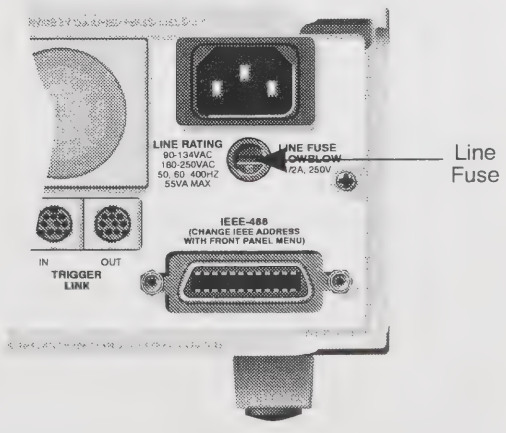


Figure 1-1
Line fuse location

NOTE

If the power line fuse continues to blow, a circuit malfunction exists and must be corrected. Refer to the troubleshooting section of this manual for assistance.

Table 1-1
Power line fuse

Size	Rating	Keithley Part No.
5 × 20mm	250V, ½A, Slo-Blo	FU-71

1.3 Current fuse replacement

Each AMPS input (front and rear) has its own current fuse. When replacing a current fuse, use the type specified in Table 1-2.

Table 1-2
Current fuse

Size	Rating	Keithley Part No.
5 × 20mm	250V, 2A, Normal-Blo	FU-48

WARNING

Disconnect the instrument from the power line and remove all test leads (front and rear).

1.3.1 Front AMPS input fuse

The front panel AMPS jack functions as the AMPS input terminal and as the carrier for the AMPS fuse (see Figure 1-2). Perform the following steps to replace the fuse:

1. Push in the AMPS input jack and turn counterclockwise until the spring loaded fuse carrier releases from the fuse holder.
2. Pull out the fuse carrier and replace the fuse with the type specified in Table 1-2.

CAUTION

To prevent instrument damage, use only the type specified in Table 1-2.

3. Re-install the fuse carrier.

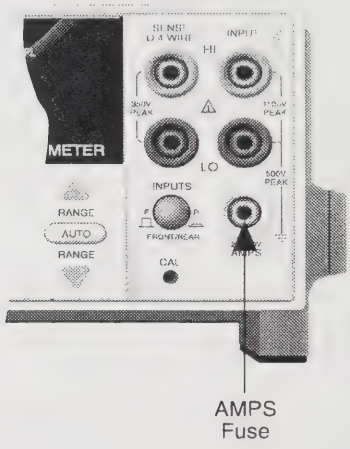


Figure 1-2
Front AMPS input fuse location

1.3.2 Rear AMPS input fuse

The rear AMPS input fuse is located just below the AMPS input jack (see Figure 1-3). Perform the following steps to replace the fuse:

1. Insert a bladed screwdriver into the slot of the fuse carrier.
2. While pushing in, turn the screwdriver counterclockwise until the spring loaded fuse carrier releases from the fuse holder.
3. Pull out the fuse carrier and replace the fuse with the type specified in Table 1-2.

CAUTION

To prevent instrument damage, use only the fuse type specified in Table 1-2.

4. Re-install the fuse carrier.

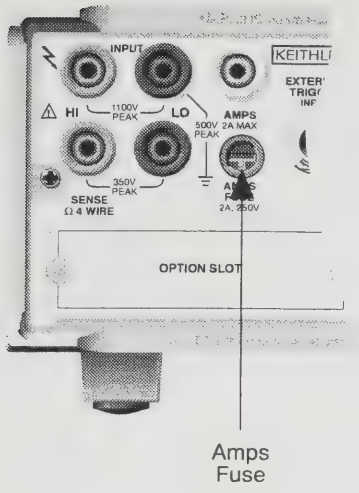


Figure 1-3
Rear AMPS input fuse location

1.4 Fan filter cleaning

The filter for the cooling fan requires periodic cleaning to maintain proper ventilation. The fan filter is accessible from the rear panel. Perform the following steps to remove the filter for cleaning:

1. While facing the rear panel, locate the lower right-hand corner of the filter cover plate.
2. At this corner, place a thin-bladed screwdriver between the cover plate and the rear panel and gently pry the filter assembly away from the chassis.

The filter element is permanently fixed to the cover plate. Do not attempt to remove the filter element from the cover plate.

WARNING

Exercise care when handling the filter assembly. The filter element is a metal screen with sharp edges that could cause injury if not handled carefully.

The filter element is made of a rugged metal screen allowing the use of any type cleaning solution to clean it. A small metal brush can be used to remove dirt and debris. After cleaning the filter, rinse thoroughly with water. Make sure the filter assembly is completely dry before re-installing it.

1.5 Firmware updates

It is possible that you may receive a firmware update from Keithley to enhance operation and/or fix "bugs". The firmware program for the main microprocessor is contained in U611 (EPROM). A socket is used on the pc board for this device to make replacement relatively easy.

The replacement procedure requires that the case cover be removed. Also, this surface mount, static-sensitive device requires special handling. As a result, the firmware update should only be performed by qualified service personnel. The procedure to replace the firmware (U611) is contained in paragraph 3.8.

2

Troubleshooting

WARNING

The information in this section is intended for qualified service personnel. Some of these procedures may expose you to hazardous voltages. Do not perform these hazardous procedures unless you are qualified to do so.

2.1 Introduction

This section of the manual will assist you in troubleshooting the Model 2001. Included are self-tests, test procedures, troubleshooting tables and circuit descriptions. It is left to the discretion of the repair technician to select the appropriate tests and documentation needed to troubleshoot the instrument.

This section is arranged as follows:

2.2 **Repair considerations** — Covers some considerations that should be noted before making any repairs to the Model 2001.

2.3 **Power-on test** — Describes the tests that are performed on its memory elements every time the instrument is turned on.

2.4 **Front panel tests** — Provides the procedures to test the functionality of the front panel keys and the display.

2.5 **Built-In tests** — Provides the procedures to test and exercise the various circuits on the digital board, analog board and A/D converter boards.

2.6 **Diagnostics** — Explains how to use the Diagnostics test mode of the Model 2001. In general, Diagnostics locks-up the instrument in various states of operation. With the instrument in a static state, you can then check the state of the various logic levels on the control registers and signal trace through the unit.

2.7 **R1_STB and R2_STB registers** — Provides shift register bit patterns for the basic measurement functions and ranges.

2.8 **Display board checks** — Provides display board checks that can be made if Front Panel Tests fail.

2.9 **Power supply checks** — Provides power supply checks that can be made if the integrity of the power supply is questioned.

2.10 **Documentation** — Provides support documentation for the various troubleshooting tests and procedures. Included is some basic circuit theory for the display board and power supply, and support documentation for Built-in Test.

2.2 Repair considerations

Before making any repairs to the Model 2001, be sure to read the following considerations.

CAUTION

The PC-boards are built using surface mount techniques and require specialized equipment and skills for repair. If you are not equipped and/or qualified, it is strongly recommended that you send the unit back to the factory for repairs or limit repairs to the pc-board replacement level (see following NOTE).

Without proper equipment and training, you could damage a PC-board beyond repair.

NOTE

For units that are out of warranty, completely assembled PC-boards can be ordered from Keithley to facilitate repairs.

1. Repairs will require various degrees of disassembly. However, it is recommended that the Front Panel Tests (paragraph 2.4) and Built-In-Test (paragraph 2-5) be performed prior to any disassembly. The disassembly instructions for the Model 2001 are contained in Section 3 of this manual.
2. Do not make repairs to surface mount pc-boards unless equipped and qualified to do so (see previous CAUTION).
3. When working inside the unit and replacing parts, be sure to adhere to the handling precautions and cleaning procedures explained in paragraph 3.2.
4. Many CMOS devices are installed in the Model 2001. These static-sensitive devices require special handling as explained in paragraph 3.3.
5. Anytime a circuit board is removed or a component is replaced, the Model 2001 will have to be recalibrated.

2.3 Power-on test

During the power-on sequence, the Model 2001 will perform a checksum test on its EPROM (U611 and U618) and test its RAM (U608, U609, and U610. If one of these tests fail the instrument will lock up.

2.4 Front panel tests

There are two Front Panel Tests; one to test the functionality of the front panel keys and one to test the display. In the event of a test failure, refer to paragraph 2.8 to troubleshoot the display board.

2.4.1 KEYS Test

The KEYS test allows you to check the functionality of each front panel key. Perform the following steps to run the KEYS test.

1. Display the MAIN MENU by pressing the MENU key.
2. Use the ◄ or ► key to place the cursor on TEST and press ENTER to display the SELF-TEST MENU.
3. Place the cursor on FRONT-PANEL-TESTS and press ENTER to display the following menu:

```
FRONT PANEL TESTS
KEYS   DISPLAY-PATTERNS
```

4. Place the cursor on KEYS and press ENTER to start the test. When a key is pressed, the label name for that key will be displayed to indicate that it is functioning properly. When the key is released, the message "No keys pressed" is displayed.
5. Pressing EXIT tests the EXIT key. However, the second consecutive press of EXIT aborts the test and returns the instrument to the SELF-TEST MENU. Keep pressing EXIT to back out of the menu structure.

2.4.2 DISPLAY PATTERNS Test

The display test allows you to verify that each pixel and annunciator in the vacuum fluorescent display is working properly. Perform the following steps to run the display test:

1. Display the MAIN MENU by pressing the MENU key.
2. Use the ◄ or ► key to place the cursor on TEST and press ENTER to display the SELF-TEST MENU.
3. Place the cursor on FRONT-PANEL-TESTS and press ENTER to display the following menu:

FRONT PANEL TESTS
KEYS DISPLAY-PATTERNS

4. Place the cursor on DISPLAY-PATTERNS and press ENTER to start the display test. There are five parts to the display test. Each time a front panel key (except EXIT) is pressed, the next part of the test sequence is selected. The five parts of the test sequence are as follows:
   A. Checkerboard pattern (alternate pixels on) and all annunciators.
   B. Checkerboard pattern and the annunciators that are on during normal operation.
   C. Horizontal lines (pixels) of the first digit are sequenced.
   D. Vertical lines (pixels) of the first digit are sequenced.
   E. Each digit (and adjacent annunciator) is sequenced. All the pixels of the selected digit are on.
5. When finished, abort the display test by pressing EXIT. The instrument returns to the SELF-TEST MENU. Keep pressing EXIT to back out of the menu structure.

2.5 Built-in test

BUILT-IN TEST is used to test and exercise various circuits and components on the digital board, analog board and A/D converter board. The Built-In Tests are listed in Table 2-1. Many of the tests are actual pass/fail type tests, while others are circuit exercises that are used for subsequent tests. Each Built-In Test can be run manually. After a test is manually run, operation is "frozen" to allow the technician to troubleshoot the circuit. Troubleshooting documentation for each Built-In Test is provided in paragraph 2.10.3.

Table 2-1
Built-in-test summary

Test	Circuit tested/exercised
100 Series	Memory:
100.1	EPROM
101 Series	Memory:
101.1	RAM
102 Series	Memory:
102.1	E^2PROM
103 Series	Digital I/O:
103.1 - 103.4	Digital Output
103.5	Digital Input
104 Series	IEEE-488 Bus:
104.1	Handshake
104.2	Data
105 Series	Triggers:
105.1 - 105.6	System Trigger Bus
105.7	External Trigger /Voltmeter Complete
105.8	Group Execute Trigger (GET)
105.11 - 105.18	Trigger Shorts
200 Series	A/D Converter:
200.1	A/D Zero
200.2	A/D Noise
200.3	FAST Circuit
200.4	x10 Line Cycle Integration
200.5	x0.1 Line Cycle Integration
200.6	x0.02 Line Cycle Integration
200.7	x0.01 Line Cycle Integration
201 Series	Calibration:
201.1	Test Cal Zero
201.2	7V Reference
201.3	1.75V Reference
300 Series	A/D Multiplexer (MUX), A/D Buffer:
300.1	7V Reference, x1.5 Gain
300.2	1.75V Reference, x5 Gain
300.3	0V Reference, x50 Gain
301 Series	Input Buffer:
301.1	Front End (FE) Zero
301.2	Divide by 100

Table 2-1 (cont.)
Built-in-test summary

Test	Circuit tested/exercised
302 Series	Ohms:
302.1	Zero Reference Measurement (for next test)
302.2	Open Circuit Ohms and Ohms Protection
303 Series	Input Path:
303.1	Zero Reference Measurement (for next test)
303.2	Open Circuit Ohms and Ohms Protection
303.3	Front End (FE) Zero Protection
304 Series	Ohms Sources:
304.1	Zero Reference Measurement (for tests 304.2 - 304.7)
304.2	0.98mA and 9.2mA Ohms Sources
304.3	89µA and 0.98mA Ohms Sources
304.4	7µA and 89µA Ohms Sources
304.5	770nA and 7µA Ohms Sources
304.6	70nA and 770nA Ohms Sources
304.7	4.4nA and 770nA Ohms Sources
305 Series	Input Divider:
305.1	Zero Reference Measurement (for next test)
305.2	Divide by 100
306 Series	Switching:
306.1	Ohms Cal Switch
307 Series	Cal Divider:
307.1	Zero Reference Measurement (for next test)
307.2	A/D MUX /10
307.3	A/D MUX /Buffer (x-0.5)

Table 2-1 (cont.)
Built-in-test summary

Test	Circuit tested/exercised
308 Series	4-Digit Mode:
308.1	A/D MUX 4-Digit Signal Path
308.2	A/D MUX 4-Digit Zero Path
309 Series	Amps:
309.1	200µA Range
309.2	2mA Range
309.3	20mA Range
309.4	Reference Measurement (for tests 309.5 and 309.6)
309.5	200mA Range
309.6	2A Range
310 Series	Protection:
310.1	Amps Protection
400 Series	Digital-to-Analog Converter (DAC):
400.1	-4.21V Output
400.2	-2.08V Output
400.3	-0.001V Output
400.4	+2.25V Output
400.5	+4.33V Output
401 Series	Signal Switching:
401.1	Zero Cal Switch
402 Series	Signal Switching:
402.1	Frequency Switch
403 Series	Signal Switching:
403.1	Ground Switch
404 Series	Absolute Value (x1 Gain):
404.1	-Full Scale DAC Output
404.2	-Half Scale DAC Output
404.3	Zero DAC Output
404.4	+Half Scale DAC Output
404.5	+Full Scale DAC Output

Table 2-1 (cont.)
Built-in-test summary

Test	Circuit tested/exercised
405 Series	Absolute Value (x10 Gain):
405.1	Gain Comparison (Large +DAC Output)
405.2	Gain Comparison (Large +DAC Output)
405.3	Gain Comparison (Small +DAC Output)
405.4	Gain Comparison (Small +DAC Output)
405.5	Gain Comparison (Small -DAC Output)
405.6	Gain Comparison (Small -DAC Output)
405.7	Gain Comparison (Large -DAC Output)
405.8	Gain Comparison (Large -DAC Output)
406 Series	Test Buffer:
406.1	Measure DAC Output (for test 406.6)
406.2	Test Buffer Output (-1.13V)
406.3	Read Test Buffer (for test 406.6)
406.4	Read DAC Output (for test 406.6)
406.5	Test Buffer Output (-0.01V)
406.6	Voltage Comparisons
407 Series	Front End:
407.1	2V Range
407.2	200V Range
407.3	750V Range
408 Series	/200 Correction Factor:
408.1	Circuit Setup (for next test)
408.2	Signal Stored (for next test)
408.3	Setup (for test 408.5) and Measurement (for test 408.6)
408.4	Same as Test 408.3 but no measurement.
408.5	Signal Stored (for next test)
408.6	Signal Comparisons

Table 2-1 (cont.)
Built-in-test summary

Test	Circuit tested/exercised
409 Series	/750 Correction Factor:
409.1	Circuit Setup (for next test)
409.2	Signal Stored (for next test)
409.3	Setup (for test 409.5) and Measurement (for test 409.6)
409.4	Same as Test 409.3 but no measurement.
409.5	Signal Stored (for next test)
409.6	Signal Comparisons
410 Series	Converter:
410.1	TRMS Converter
411 Series	Filters:
411.1	TRMS Filter
411.2	Variable Gain Amplifier Filter
412 Series	Switching:
412.1	AC Amps Switch

Typical Way To Use BUILT-IN-TEST

1. Run the AUTOMATIC Built-In-Test as explained in paragraph 2.5.1 and note the first (lowest numbered) test that has failed. You should always address the lowest numbered test failure first because that failure could cause subsequent tests to fail.
2. Familiarize yourself with the failed circuit. Documentation for the Built-In Tests are provided in paragraph 2.10.3. Be sure to read the documentation for the complete series. For example, if test 200.4 fails, read the documentation for all 200 series tests (200.1 through 200.7). Note that the documentation directs you to the appropriate schematic(s) for the circuit.
3. Manually run the test that failed as explained in paragraph 2.5.2. Keep in mind that many of the pass/fail type tests require that one or more circuit exercise tests be run first. Using the manual step looping mode will "freeze" instrument operation after a test is run.
4. After manually running the test, use the test documentation and your troubleshooting expertise to locate the problem.

5. After repairing the instrument, start again at step 1 to check the integrity of the repair and to see if there are any other failures.

2.5.1 AUTOMATIC Testing

1. Display the MAIN MENU by pressing the MENU key.
2. Use the ◄ or ► key to place the cursor on TEST and press ENTER to display the SELF-TEST MENU.
3. Place the cursor on BUILT-IN-TEST and press ENTER to display the following menu:

```
BUILT-IN TEST
AUTOMATIC  MANUAL
```

4. Place the cursor on AUTOMATIC and press ENTER. The following prompt is displayed:

```
CONTINUOUS REPEAT?
NO  YES
```

In the non-repeat mode (NO), the testing process stops after all tests have been performed one time. In the continuous repeat mode (YES), the testing process loops around and repeats indefinitely until the EXIT key is pressed to stop the tests.

5. Place the cursor on the desired repeat mode selection (NO or YES) and press ENTER to start the testing process. The instrument displays the number of the test being run. An "A" on the display indicates that the tests are being run automatically in the non-repeat mode. An "AC" indicates that the tests are being run automatically in the continuous repeat mode. If a failure occurs, a star (*) appears at the right hand end of the display and remains on for the remainder of the tests.
6. If the non-repeat mode is selected, the testing process automatically stops when all the tests have been performed. If the continuous repeat mode is selected, you will have to manually stop the testing process by pressing EXIT. When EXIT is pressed, all the tests in a series already started will be allowed to finish.

When the testing process stops, the following message is displayed:

```
All tests complete *
Press ENTER to review or EXIT
```

The star (*) is only displayed if a failure occurs.

7. If all the tests passed (no star displayed), use the EXIT key to back out of the menu structure. Otherwise, press ENTER to display the test number of the first failure. You can display any additional failures by using the ◄ and ► keys. With a failed test displayed, pressing the INFO key provides an abbreviated description of the failure. Paragraph 2.10 provides detailed documentation for troubleshooting the defective circuit. When finished, use EXIT to back out of the menu structure.

2.5.2 MANUAL Testing

1. Display the MAIN MENU by pressing the MENU key.
2. Use the ◄ or ► key to place the cursor on TEST and press ENTER to display the SELF-TEST MENU.
3. Place the cursor on BUILT-IN-TEST and press ENTER to display the following menu:

```
BUILT-IN TEST
AUTOMATIC  MANUAL
```

4. Place the cursor on MANUAL and press ENTER to display the currently selected test series number.

Test number: 100

This test number indicates that the 100 series tests can be performed. In this case there is only one test; test 100.1.

5. Use the ◄ or ► to display the desired test series number. For example, if you wish to run test 200.5, display the series 200 test number.

Test number: 200

6. With the desired test series number displayed, press ENTER. The following menu displayed:

```
SELECT LOOPING
SINGLE  CONTINUOUS  STEP
```

7. Place the cursor on the desired looping selection and press ENTER.
   A. SINGLE Looping performs all the tests in the specified series. The instrument displays the number of the test being run, and an "M" is dis-

played to indicate that the tests are being run in the manual single looping mode. If a failure occurs, a star (*) appears at the right hand end of the display and remains on for the remainder of the tests in the series. This testing process automatically stops after the last test in the series is completed. This test process can also be stopped by pressing EXIT. When EXIT is pressed, any test in process will be allowed to finish before aborting the testing process.

B. CONTINUOUS looping continuously repeats all the tests in the specified series until the testing process is manually stopped. During testing, the "MC" message is displayed to indicate that tests are being run in the manual continuous looping mode. If a failure occurs, a star (*) appears at the right hand end of the display and remains on for the remainder of the tests in the series. This test process can be stopped by pressing EXIT. When EXIT is pressed, any test in process will be allowed to finish before aborting the testing process.

C. STEP looping is used to perform one test at a time. Each press of the ENTER key performs the displayed test. The "MS" message is displayed to indicate that tests are being run in the manual step looping mode. If a failure occurs, a star (*) appears at the right hand end of the display and remains on for the remainder of the tests in the series. The instrument automatically aborts the testing process after the last test in the series is run. If you do not wish to run all the tests in the series, simply press EXIT after the desired test is run.

8. After the testing process is stopped, the following message is displayed:

   All tests complete *
   Press ENTER to review or EXIT

   The star (*) is only displayed if a failure occurs.

9. In the event of no test failures, press any key to return to the BUILT-IN TEST menu. If you wish to run more tests, repeat steps 4 through 8.

   In the event of a failure, press ENTER to display the first test that failed. Other test failures can be displayed by using the ◄ and ► keys. The INFO key can be used to provide a brief summary of each displayed test failure. Paragraph 2.10.3 provides detailed documentation for troubleshooting the defective circuit. When finished, press EXIT to return to the BUILT-IN TEST menu. If you wish to run more tests, repeat steps 4 through 8.

10. When finished with BUILT-IN TEST, use the EXIT key to back out of the menu structure.

2.6 Diagnostics

The Model 2001 has diagnostic test modes which allow you to "freeze" instrument operation to allow you to check logic levels on the DC_STB control registers (U303, U300, U800 and U801). The known bit pattern at these registers can then be used for signal tracing through the unit. Table 2-10 provides a brief description of each register bit.

Perform the following steps to use DIAGNOSTICS:

1. Select the desired function and range to be checked. Note that there are no range selections for FREQ and TEMP.
2. Display the MAIN MENU by pressing the MENU key.
3. Using the ◄ or ► key to place the cursor on TEST and press ENTER to display the SELF-TEST MENU.
4. Place the cursor on DIAGNOSTICS and press ENTER. The first diagnostic test mode (Signal Phase or Ohms Sense High) is selected (displayed).
5. Perform the following steps to determine the bit pattern at the control registers:
   A. Refer to one of the following DIAGNOSTIC Test Modes tables to determine the bit pattern designator (A through X) for the selected function/range:

      Table 2-2 — All functions except Ω4

      Table 2-3 — Ω4 function; 20Ω and 200Ω ranges

      Table 2-4 — Ω4 function, 2kΩ, 20kΩ and 200kΩ ranges

   B. Once the bit pattern designator is determined, use Table 2-5 to determine the logic state of each register bit.

      Example: Assume the 20VDC range is selected and the instrument is in the "Signal Phase" of DIAGNOSTICS. From Table 2-2, the bit pattern designator is C. Table 2-5 provides the logic states for bit pattern C.
6. Use the cursor keys to select the other diagnostic test modes. The ► key scrolls forward through the

test modes and the ◄ key scrolls backward. Again, use the appropriate tables to determine the bit pattern at the control registers.

7. When finished, press EXIT three times to back out of the menu structure and return to the normal measurement mode of operation.
8. If you wish to check another function/range, repeat steps 1 through 7.

Table 2-2
DIAGNOSTICS test modes (all functions except Ω4)

Test mode	Selected function	Selected range	Bit pattern designator*
Signal Phase	DCV	200mV 2V, 200V 20V 1000V	A B C D
	ACV, ACI and FREQ	All	E
	DCI	All	F
	Ω2	20Ω, 200Ω 2kΩ-200MΩ 1GΩ	G H I
	TEMP RTD (open input)	—	H
	TEMP TC	—	B
7V div by 1 * 1	All (except Ω4)	All	J
7V div by 1 * 1.5	All (except Ω4)	All	K
2V div by 1 * 5	All (except Ω4)	All	L
0V div by 1 * 1	All (except Ω4)	All	M
0V div by 1 * 5	All (except Ω4)	All	N
0V div by 1 * 50	All (except Ω4)	All	O
0V div by 1 * 1.5	All (except Ω4)	All	P
FE zero for 200mV	All (except Ω4)	All	Q
FE zero for 2V	All (except Ω4)	All	R

*Bit patterns are provided in Table 2-5.

Table 2-3
DIAGNOSTICS test modes (Ω4 function; 20Ω and 200Ω ranges)

Test mode	Bit pattern designator*
Ohms sense high	G
7V div by 1 * 1	P
7V div by 1 * 1.5	Q
2V div by 1 * 5	R
0V div by 1 * 1	S
0V div by 1 * 5	T
0V div by 1 * 50	U
0V div by 1 * 1.5	V
Ohms sense minus	W
FE zero for 2V	X

*See Table 2-5 for bit patterns.

Table 2-4
DIAGNOSTICS test modes (Ω4 function; 2kΩ thru 200kΩ ranges)

Test mode	Bit pattern designator*
Ohms sense high	H
7V div by 1 * 1	P
7V div by 1 * 1.5	Q
2V div by 1 * 5	R
0V div by 1 * 1	S
0V div by 1 * 5	T
0V div by 1 * 50	U
0V div by 1 * 1.5	V
FE zero for 200mV	W
Ohms sense minus	X

*See Table 2-5 for bit patterns.

Table 2-5
DIAGNOSTICS bit patterns (DC_STB registers)

Bit pattern	Registers																													
	U303								U300								U800								U801							
	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1
A	X	X	1	1	1	0	1	1	0	1	1	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
B	X	X	1	1	1	1	0	1	0	1	1	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
C	X	X	1	1	1	1	1	1	0	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
D	X	X	1	1	1	1	1	0	0	1	1	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
E	X	X	1	0	1	1	0	1	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
F	X	X	0	1	1	0	1	1	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
G	X	X	1	1	1	0	1	1	0	1	1	1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
H	X	X	1	1	1	1	0	1	0	1	1	1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
I	X	X	1	1	1	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
J	X	X	1	1	1	1	1	0	0	1	1	1	1	0	1	1	0	1	1	0	1	0	1	0	1	0	0	0	0	1	0	0
K	X	X	1	1	1	1	1	1	0	1	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
L	X	X	1	1	0	1	0	1	0	1	1	1	1	1	1	1	0	1	1	0	1	0	1	0	1	0	0	0	0	1	0	0
M	X	X	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
N	X	X	1	1	1	1	0	1	0	0	1	1	1	1	1	1	0	1	1	0	1	0	1	0	1	0	0	0	0	1	0	0
O	X	X	1	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
P	X	X	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	1	1	0	1	0	1	0	1	0	0	0	0	1	0	0
Q	X	X	1	1	1	0	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
R	X	X	1	1	1	1	0	1	1	1	1	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	0	0	0	1	0	0
S	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0	1
T	0	0	1	1	1	1	0	1	0	0	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1	0	1	0	1	1	1	0
U	0	0	1	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0	1
V	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1	0	1	0	1	1	1	0
W	0	0	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	1	1	0	1	0	1	0	0	1	0	1	0	1	0	1
X	0	0	1	1	1	1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	1	1	0

2.7 R1_STB and R2_STB shift registers

Table 2-6 and Table 2-7 are provided to allow you to check logic levels on the R1_STB and R2_STB shift registers (U302, U305, U307, U501, U530, U500 and U505) for each basic measurement function (DCV, ACV, DCI, ACI, Ω2 and Ω4) and range. The known bit pattern at these registers can then be used for signal tracing through the unit. Tables 2-11 and Table 2-12provide a brief description of each register bit.

To use these tables, simply place the instrument in the designated function and range and check the output of the shift registers for the indicated bit pattern. The bit patterns in these tables assume the following conditions:

NPLC > 0.01
AC Type = RMS or Average
Offset Compensated Ohms = Off
Current Measurement Mode = Normal (No In-Circuit I)

Table 2-6
Bit patterns for R1_STB registers

Function	Range	Registers																							
		U302								U305								U307							
		Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1
DCV	200mV-20V	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0	1	1	0	1	0
	200V, 1000V	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
ACV	All	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	1	0
DCI	200µA	0	1	1	1	1	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	2mA	0	1	1	1	0	1	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	20mA	0	1	1	0	1	1	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	200mA	0	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	2A	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
ACI	200µA	0	1	1	1	1	0	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	2mA	0	1	1	1	0	1	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	20mA	0	1	1	0	1	1	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	200mA	0	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
	2A	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	0	1	1	0	1	0
Ω2	20Ω	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	1	0	0	0
	200Ω, 2kΩ	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	1	0	0	1
	20kΩ	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	1	0	1	0
	200kΩ	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	1	0	1	1
	2MΩ	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	1	1
	20MΩ	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	1	0	1	1
	200MΩ, 1GΩ	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	1	0	1	1
Ω4	20Ω	0	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	1	1	0	1	1	1	0	0
	200Ω, 2kΩ	0	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	1	1	0	1	1	1	0	1
	20kΩ	0	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	1	1	0	1	1	1	1	0
	200kΩ	0	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	1	1	0	1	1	1	1	1

Table 2-7
Bit patterns for R2_STB registers

Function	Range	Registers															
		U501								U530							
		Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1
DCV	All	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
ACV	200mV	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0
	2V	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0
	20V	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0
	200V	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0
	750V	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0
DCI	All	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
ACI	All	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0
Ω2, Ω4	All	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0

Range	Range	Registers															
		U500								U505							
		Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1
DCV	All	1	0	1	0	0	0	1	1	0	0	0	0	0	1	1	1
ACV	200mV	1	1	1	0	1	1	0	1	1	0	0	1	1	1	1	1
	2V	1	1	1	0	1	0	0	1	1	0	1	1	1	1	1	1
	20V	1	1	1	0	1	1	1	0	0	0	0	1	1	1	1	0
	200V	1	1	1	0	1	1	1	0	0	0	0	1	1	1	1	0
	750V	1	1	1	0	1	0	1	0	0	0	0	1	1	1	1	0
DCI	All	1	0	1	0	0	1	1	1	0	0	0	1	1	1	1	1
ACI	All	1	1	1	0	1	1	1	1	0	1	0	0	1	1	1	1
Ω2, Ω4	All	1	0	1	0	0	0	1	1	0	0	0	0	0	1	1	1

2.8 Display board checks

If the FRONT PANEL TESTS (paragraph 2.4) indicate that there is a problem on the display board, use Table 2-8.

Circuit theory for the display is provided in paragraph 2.9.1.

2.9 Power supply checks

Power supply problems can be checked out using Table 2-9.

Table 2-8
Display board checks

Step	Item/component	Required condition	Remarks
1	FRONT PANEL TESTS	Verify that all pixels operate	Use SELF-TEST MENU selection
2	P1033, pins 4, 6, 14 and 16	5VAC, ±0.3VAC	VFD filament
3	P1033, pin 5	+5V, ±5%	Digital +5V supply
4	P1033, pin 9	+60V, ±10%	VFD +60V supply
5	P1033, pin 12	Goes low briefly on power-up, then goes high	Microcontroller RESET line
6	P1033, pin 2	4MHz square wave	Controller 4MHz clock
7	P1033, pin 8	Pulse train every 1msec	Control from main processor
8	P1033, pin 10	Brief pulse train when front panel key is pressed	Key down data sent to main processor.

Table 2-9
Power supply checks

Step	Item/component	Required condition	Remarks
1	F100 line fuse	Check continuity	Remove to check
2	Line power	Plugged into live receptacle, power on	Check for correct power up sequence
3	U108, pin 3	+5V, ±5%	Reference to Common 3
4	U107, pin 3	+15V, ±0.75V	Reference to COM
5	U102, pin 3	-15V, ±0.75V	Reference to COM
6	CR109, +BS	+34V to +38V	Reference to Common 3
7	CR110, -BS	-34V to -38V	Reference to Common 3
8	U103, pin 3	~+18V	Reference to Isolated Common
9	U103, pin 2	+8V	Reference to Isolated Common
10	U619, +5VC	+5V, ±5%	Reference to Digital Common
11	U629, pin 3`	+5V, ±5%	Reference to Digital Common

2.10 Documentation

The following information is provided to support the troubleshooting tests and procedures previously covered in this section of the manual. Figure 2-1 provides an overall block diagram of the Model 2001 showing the major circuit groups. Most circuits in the Model 2001 are tested and/or exercised by Built-in Test. A short description for each of these tests explains how that particular circuit operates. The display board and the power supply are not tested by Built-in Test. Thus, some basic theory is provided for these circuits in paragraphs 2.10.1 and 2.10.2.

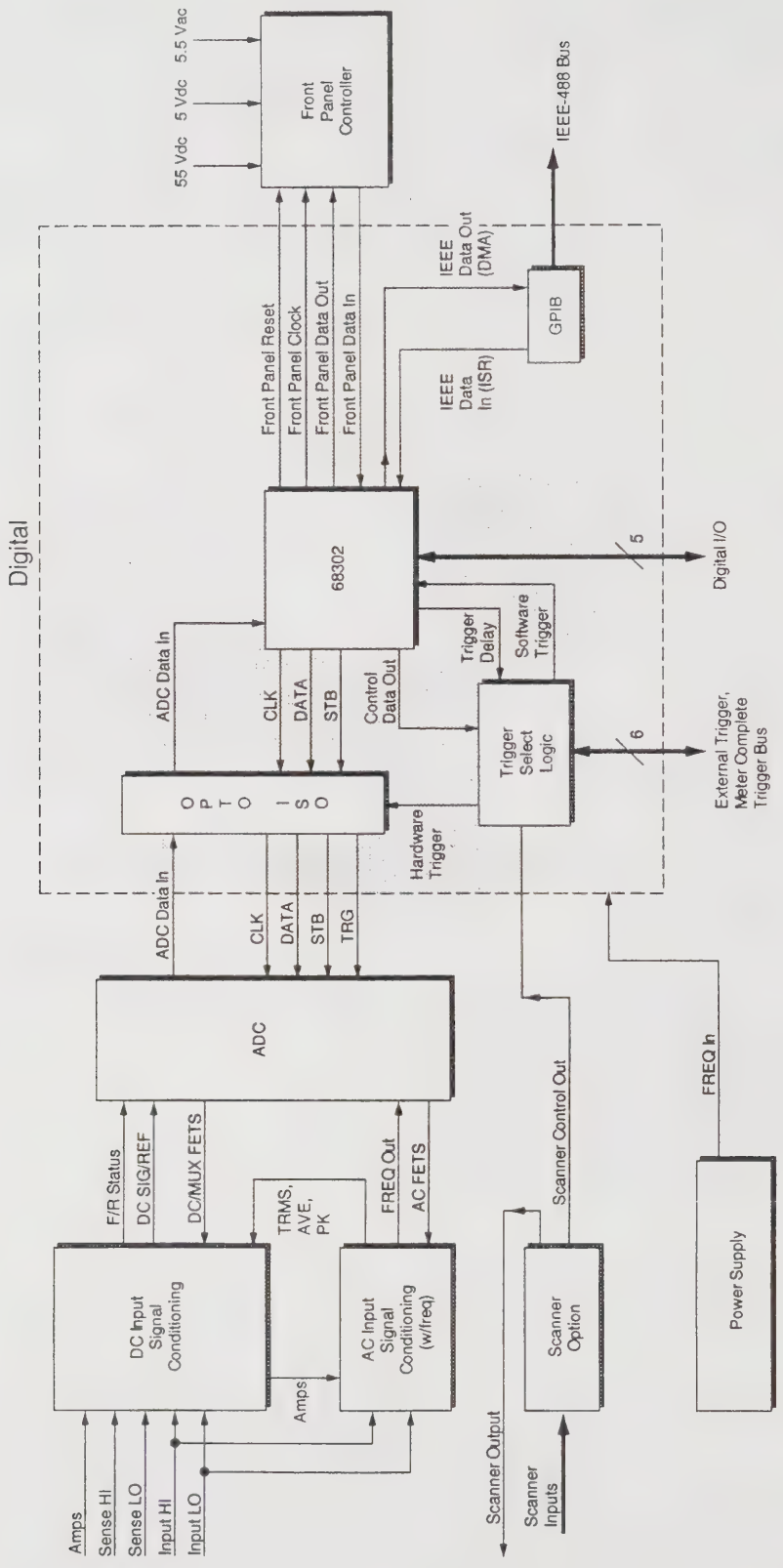


Figure 2-1
Model 2001 overall block diagram

2.10.1 Display board circuit theory

The following information provides some basic circuit theory that can be used as an aide to troubleshoot the display and keyboard.

Display microcontroller

U902 is the display microcontroller that controls the VFD (vacuum fluorescent display) and interprets key data. The microcontroller has four peripheral I/O ports that are used for the various control and read functions.

Display data is serially transmitted to the microcontroller from the digital board via the TXB line to the microcontroller PD0 terminal. In a similar manner, key data is serially sent back to the digital board through the RXB line via PD1. The 4MHz clock for the microcontroller is generated on the digital board.

Vacuum fluorescent display

DS901 is the VFD (vacuum fluorescent display) module, which can display up to 49 characters. Each character is organized as a 5×7 matrix of dots or pixels and includes a long under-bar segment to act as a cursor.

The display uses a common multiplexing scheme with each character refreshed in sequence. U903 and U904 are the grid drivers, while U901 and U905 are the dot drivers. Note that dot driver and grid driver data is serially transmitted from the microcontroller (PD3 and PC1).

The VFD requires both +60VDC and 5VAC for the filaments. These VFD voltages are supplied by U625, which is located on the digital board.

Key matrix

The front panel keys (S901-S931) are organized into a row-column matrix to minimize the number of microcontroller peripheral lines required to read the keyboard. A key is read by strobing the columns and reading all rows for each strobed column. Key down data is interpreted by the display microcontroller and sent back to the main microprocessor using proprietary encoding schemes.

2.10.2 Power supply circuit theory

The following information provides some basic circuit theory that can be used as an aide to troubleshoot the power supply.

Pre-regulator circuit

The pre-regulator circuit regulates power to the transformer. When power is applied to the instrument, a power transformer secondary voltage (pins 12 and 13) is rectified (CR622), doubled (C624, C630, CR624 and CR625) and applied to U619 which is a +5V regulator. This +5V (+5VC) is used for the pre-regulator circuit.

The pre-regulator circuit monitors the voltage level on C611 using an integrator (U627). The voltage on C611 (typically around 7.5V) is divided by three through R712 and R713 and applied to the inverting input (pin 2) of the integrator. The +5V (+5VC) is divided by two through R706 and R708. This 2.5V reference is applied to the non-inverting input (pin 3) of the integrator.

When the voltage on the inverting input of the integrator is less than the 2.5V reference on the non-inverting input, the integrator output ramps in the positive direction. This positive ramp turns on Q608 which pulls the CONT line low to digital common. With CONT connected to common, current flows through the photodiode of U100 and generates a positive voltage at the gate of FET Q528. As Q528 turns on, the 470Ω resistor (R100) becomes shunted and results in less effective resistance to the transformer. The resultant increase in current (power) will increase the voltage on C611.

Conversely, when the voltage on the inverting input of the integrator is more than the 2.5V reference, the integrator output ramps in the negative direction and begins to turn Q608 off. This will decrease current through U100, decrease the positive voltage on Q528 and thus, increase the effective resistance to the transformer. The resultant decrease in current (power) will decrease the voltage of C611.

This constant regulation of effective resistance in series with the transformer regulates the power delivered to the instrument.

Line voltage (110V/220V) selection circuit

This circuit automatically selects the proper power line voltage setting for the instrument. The line selection circuit derives its power from the AC1 and AC2 lines on the primary side of the transformer. Rectifier CR101 applies approximately +18V to regulator U103. The output of U103 provides the +8V for the line voltage selection circuit and the HI/LO voltage control circuit.

U106 is a comparator that has a +4V reference (via voltage divider R125 and R126) applied to its non-inverting input. The inverting input monitors the voltage on C111. When the voltage at the inverting input is greater than 4V, the output of U106 goes low and turns on FET Q103. With Q103 on, +8V will be applied to the +RELAY1 line which energizes relay K101 to select the 110V setting. Conversely, when the voltage at the inverting input is less than 4V, the output of U106 goes high and turns off Q103. With Q103 off, the +8V is removed from K101 and thus, the line voltage setting defaults to 220V.

The AC power line is tied to C111 through CR104, R227 and R114 via control line ACL. When the AC power line voltage is less than approximately 135VAC, sufficient charge remains on C111 to keep the inverting input of U106 above 4V to ultimately energize K101 (110V setting). When the AC power line voltage is greater than approximately 18VAC, charge will be pulled from C111 dropping the voltage at the inverting input of the comparator to less than 4V. This will de-energize K101 (220V setting).

HI/LO voltage control circuit

This circuit automatically selects the appropriate HI/LO setting for the available power line voltage. During power-up, the line voltage is rectified (CR100), divided (R103 and R105, or R102 and R105) and applied to the base of Q101.

If the voltage level at the base of Q101 is high (above zener VR101), the transistor will turn on and apply power to the ISO1+ and ISO1- lines. With power applied to ISO1+ and ISO1-, U105 will turn on and allow Q105 to be forward biased. With U105 and Q105 on, TRIG of U110 will be pulled low and allow its output (OUT) to latch at +8V which will turn on FET Q102. With Q102 on, the -RELAY2 line will be connected to common, and thus energize K100 (HI setting).

If the power line voltage decreases to a low level, U105 will turn off, but the output of U110 will remain latched at +8V. However, the LOW line will be driven low turning on U109. With U109 and Q106 on, +8V will be applied to THR of U110 forcing its output (OUT) to reset to low. With the gate of Q102 low, the FET will turn off and open the relay coil circuit for K100 (LO setting).

The LOW line is controlled by comparator U628. The inverting input of the comparator is connected to the 2.5V reference. The non-inverting input monitors (via divider R709 and R711) C611. As previously explained, the typical power line voltage level will apply around 7.5V to C611. However, if the line voltage decreases such that the voltage on C611 becomes less than 6V, the voltage level on the non-inverting input of the comparator will drop below 2.5V causing its output (LOW line) to go low.

2.10.3 Built-in test documentation

The information in this paragraph provides documentation for each Built-In Test. Paragraph 2.5 explains how to use the Built-In Test.

The following documentation is provided for each Built-In Test:

1. Test Type — Some tests are pass/fail type tests while others are circuit exercises that are used for subsequent tests.
2. Failure Analysis — For pass/fail type tests, a summary is provided to explain the cause of the failure.
3. Description — Provides a description of the circuit being tested.
4. Schematic Reference — Directs you to the appropriate schematic(s) for the circuit being tested.
5. High Suspect Components — When appropriate, possible defective components and/or circuits are listed. It is left to the expertise of the repair technician to pin-point the problem.
6. Shift Registers — For tests starting with 200.1, the logic states for the control shift registers are provided. After one of these tests is manually run, you can check the registers for the correct logic levels. Tables 2-10 through 2-12 provide functional descriptions for the register bits.
7. Multiplexer — For manually run tests that exercise the multiplexer (U511), you can use Table 2-13 to check the logic levels on its control lines.

Table 2-10
DC_STB control registers

Register	Bit	Pin	Control	Description
U801	Q1	4	FAST	1 = FAST integration on A/D converter (ADC).
	Q2	5	LST_PH	1 = Normal ADC operation.
	Q3	6	FREQ_EN	1 = Normal ADC operation.
	Q4	7	I3, FREQ_LOAD	1 = Normal ADC operation.
	Q5	14	I4	Set ADC conversion rate (LSB).
	Q6	13	I5	Set ADC conversion rate.
	Q7	12	I6	Set ADC conversion rate.
	Q8	11	I7	Set ADC conversion rate.
U800	Q1	4	I8	Set ADC conversion rate.
	Q2	5	I9	Set ADC conversion rate.
	Q3	6	I10	Set ADC conversion rate.
	Q4	7	I11	Set ADC conversion rate.
	Q5	14	I12	Set ADC conversion rate.
	Q6	13	I13	Set ADC conversion rate (MSB).
	Q7	12	OHMCA	Select Ohms Cal on U325 (LSB).
	Q8	11	OHMCB	Select Ohms Cal on U325 (MSB).
U300	Q1	4	BUF, /BUF	1 = Q306 on and Q304 off.
	Q2	5	VLO2, BSCOM	0 = -8VF to VLO2, 1 = -8VF to BSCOM.
	Q3	6	/REF	0 = 7V ref to A/D Buffer (via U317).
	Q4	7	//1	0 = Input Buffer to A/D Buffer (Q308 and Q313 on).
	Q5	14	/CAL	
	Q6	13	//2	0 = Cal Divider to A/D Buffer (via U319).
	Q7	12	/ZERO	0 = -0.5 or 1.5 gain (via U319).
	Q8	11	FE ZERO, ONE SHOT	0 = Zero to A/D Buffer (via U319). 1 = Q527 and Q539 on, 0 = ONE SHOT (via U334) for PRECHARGE (Q538 on).
U303	Q1	4	/X1	0 = x1 A/D Buffer; U318 (/X1) closed.
	Q2	5	/X5	0 = x5 A/D Buffer; U318 (/X5) closed.
	Q3	6	/X50	0 = x50 A/D Buffer; U318 (/X50) closed.
	Q4	7	/2VREF	0 = 1.75V ref to A/D Buffer (via U318).
	Q5	14	/AC	0 = ACV/A to A/D Buffer (via U320).
	Q6	13	/DCA	0 = DCA to A/D Buffer (via U320).
	Q7	12	nc	x
	Q8	11	nc	x

Table 2-11
R1_STB control registers

Register	Bit	Pin	Control	Description
U307	Q1	4	OHM FA	U332 ohms range select (LSB).
	Q2	5	OHM FB	U332 ohms range select (MSB).
	Q3	6	4W OHM	0 = U323 closed, 1 = U323 open.
	Q4	7	/OHM CAL	0 = OHM CAL to A/D Buffer (via U320).
	Q5	14	/4 DIGIT	0 = BSCOM or common (via U317) to A/D Buffer (U319 closed).
	Q6	13	OHM FD	1 = U332 Inhibit (INH); all channels off.
	Q7	12	/LOV/OHM, BSCOM	1 = Q333 off, 0 = Q333 on to connect signal to BSCOM.
	Q8	11	/2M	0 = Q329 on (10MΩ range).
U305	Q1	4	4 DIGIT	0 = Common to A/D Buffer (via U317).
	Q2	5	OHM	1 = K300 closed (OHMS relay).
	Q3	6	VLO, /VLO	1 = U336 and U337 turns on Q337-Q340.
	Q4	7	HI OHM, /HI OHM	1 = Q320 and Q312 off, Q324 on.
	Q5	14	/HIV	1 = Q328 off; opens divider common.
	Q6	13	/DIVIDER, BSCOM	1 = Q525 off, 0 = Q525 on to connect divider signal to BSCOM.
	Q7	12	OHM SELECT, /4W OHM, BSCOM	0 = U323 closed and Q331 on to connect signal to BSCOM.
	Q8	11	/200M	0 = U323 closed (/16 gain for 4.4nA ohms source).
U302	Q1	4	/ACA	0 = U320 (ACA) and U522 (ACBS) closed.
	Q2	5	/ACAL	0 = U323 closed.
	Q3	6	/200μA	0 = U317 closed (1kΩ shunt).
	Q4	7	/2mA	0 = U317 closed (100Ω shunt).
	Q5	14	/20mA	0 = Q311 on (10Ω shunt).
	Q6	13	/200mA	0 = Q309 and Q307 on (1Ω shunt).
	Q7	12	/2A	0 = Q310 and Q305 on (0.1Ω shunt).
	Q8	11	nc	x

Table 2-12
R2_STB control registers

Register	Bit	Pin	Control	Description
U505	Q1	4	DCF	0 = U526 (divider) closed and U526 (ACA) open.
	Q2	5	SELFTEST	1 = Q518 off, U513 arms U503, and U522 (control pin 9) open.
	Q3	6	SELFTESTEN	1 = Arms U513 (pin 5) for SELFTEST.
	Q4	7	SHORT	0 = U526 closed (common to AC Buffer).
	Q5	14	REL1	1 = Q504 on; closes relay K502 (ACV).
	Q6	13	REL2	1 = Q519 on; closes relay K503 (SELFTEST).
	Q7	12	REL3	1 = Opens U510 and turns on Q500 which closes relay K501 (pins 4 and 5).
	Q8	11	REL4	1 = Q502 on; closes K500 (Q503 on).
U500	Q1	4	750V	0 = U526 on (/500 AC divider).
	Q2	5	ACLOW	0 = Q513 on and Q516 off, 1 = Q513 off and Q516 on.
	Q3	6	RANGE	1 = U515 closed and Q508 on (x10 rectifier).
	Q4	7	/PEAK	0 = Q533 off; disables peak circuit.
	Q5	14	/RSTPK	0 = U510 (pin 9) closed and U510 (pin 16) open.
	Q6	13	TRIG9	0 = Q520 off; increases DAC resolution (1/512).
	Q7	12	TRIGLEV	0 = U515 closed and Q542 on.
	Q8	11	SEL	0 = Hold DAC B, 1 = hold DAC A.
U530	Q1	4	TRIG8	Bit DB0 of DAC U531 (LSB).
	Q2	5	TRIG7	Bit DB1 of DAC U531.
	Q3	6	TRIG6	Bit DB2 of DAC U531.
	Q4	7	TRIG5	Bit DB3 of DAC U531.
	Q5	14	TRIG4	Bit DB4 of DAC U531.
	Q6	13	TRIG3	Bit DB5 of DAC U531.
	Q7	12	TRIG2	Bit DB6 of DAC U531.
	Q8	11	TRIG1	Bit DB7 of DAC U531 (MSB).
U501	Q1	4	SEL1	SEL1, SEL2 and SEL3 control lines
	Q2	5	SEL2	determine which MUX switch (U511)
	Q3	6	SEL3	is closed (see Table 2-13).
	Q4	7	FREQ	1 = Arms U508 and closes U522.
	Q5	14	RMS	0 = U532 (pin 9) closed and U510 open.
	Q6	13	DAC	0 = U532 (pin 1) closed; DAC V to AC Buffer.
	Q7	12	nc	x
	Q8	11	nc	x

Table 2-13
Multiplexer (U511)

MUX Control Lines			Selected Input
SEL3	SEL2	SEL1	
0	0	0	IN1; Peak output
0	0	1	IN2; Filter output
0	1	0	IN3; TRMS output
0	1	1	IN4; ACF output
1	0	0	IN5; Rectifier output
1	0	1	IN6; SELFTEST OUT
1	1	0	IN7; AMP IN output
1	1	1	IN8; Common

Memory element tests

Tests 100.1, 101.1 and 102.1 check the memory elements (ROM, RAM and E²PROM) of the Model 2001.

Test 100.1 – EPROM

Type Pass/Fail

Failure analysis Cannot properly read ROM.

Description All ROM bytes (except checksum bytes) are read, a checksum is calculated and compared to the stored checksum. Failing this test indicates that one or more ROM locations cannot be read properly.

High suspect components U611 and associated logic.

Test 101.1 – RAM

Type Pass/Fail

Failure analysis Cannot properly write to and/or read RAM.

Description This is an abbreviated version of power-on RAM testing. Memory locations are written to, and then read back. It is highly unlikely that this built-in-test will fail. A unit with faulty memory will probably fail the power-on memory test or will lock up intermittently.

High suspect components U609, U610 and associated logic.

Test 102.1 – RAM

Type Pass/Fail

Failure analysis Cannot properly read the E²PROM.

Description An attempt is made to read a byte of information from the 24C16 configuration E²PROM (U617) and an acknowledgement signal is verified. Failing this test indicates a problem with the E²PROM or associated circuitry. This is a hardware test only and does not verify the validity of configuration information stored in the E²PROM.

High suspect components U617 and associated circuitry.

Digital I/O tests

The Digital I/O on the Model 2001 consists of four open collector outputs, and one TTL-level input. Outputs originate from Port A of the 68302 microprocessor (U626), lines PA4 through PA7. PA4 drives Output #1, PA5 drives Output #2, PA6 drives Output #3 and PA7 drives Output #4. These signals are buffered by a 2596A open collector driver (U612).

The following table summarizes how the lines of Port A of the microprocessor and the IN/OUT designations of the 2596A driver correspond to the digital output lines:

Digital Output	68302 (U626) Port A	2596A (U612) IN, OUT
Output #1	PA4	IN4, OUT4
Output #2	PA5	IN3, OUT3
Output #3	PA6	IN1, OUT1
Output #4	PA7	IN2, OUT2

The single Digital Input is buffered by protection circuitry (CR619, CR626, R610, R733) and read by the 68302 at PB8.

NOTE

Digital I/O tests may fail or not be run depending on the hardware and firmware revisions of the instrument.

Test 103.1 through 103.4 – Digital output

Type Pass/Fail

Failure analysis Defective digital output port

Description These tests make use of the fact that the Port A registers of the 68302 microprocessor (U626) are bidirectional even though in normal use they are programmed as outputs only.

Diodes and resistors are configured around the 2596 driver (U612) so that Output #1 feeds back to PA5, Output #2 feeds back to PA6, Output #3 feeds back to PA7 and Output #4 feeds back to PA4.

During test 103.1, PA4 is programmed as an output and PA5 is programmed as an input. As PA4 (Output #1) is toggled from high to low, the signal is read (verified) at PA5. For test 103.2, PA5 is programmed as an output and PA6 is programmed as an input. As PA5 (Output #2) is toggled from high to low, the signal is read (verified) at PA6. Tests 103.3 and 103.4 check Outputs #3 and #4 in a similar manner.

Success of these tests assures the basic functionality of Port A, the 2596 and associated components.

Test 103.5 – Digital input

Type Pass/Fail

Failure analysis Defective digital input port.

Description This test only verifies that the digital input signal is pulled high at PB8 of the microprocessor (U626). Success of this test does not guarantee complete functionality of the input port.

IEEE-488 bus tests

The IEEE-488 interface in the model 2001 consists of the 9914 GPIB chip (U622) and the 75160 (U621) and 75161 (U623) bus drivers. The 75160 buffers the data lines (DIO1-DIO8), and the 75161 buffers the bus handshake lines and other control signals. The circuitry to test these components is contained in the 5064 ASIC (U618).

Test 104.1 – Handshake

Type Pass/Fail

Failure analysis Cannot properly perform an IEEE-488 handshake.

Description Circuitry in the 5064 (U618) is set up to simulate an IEEE-488 handshake. Bytes are written to the 9914 (U622) Data Out register and the interrupt status register is checked to verify that a Byte-Out handshake is completed.

These tests verify the basic functionality of the 9914, 75161 and the handshake portion of the ASIC (Signals BNRFD, BNDAC, and BDAV).

High suspect components U618, U622 and U623.

Test 104.2 – Data

Type Pass/Fail

Failure analysis Cannot properly write data to the 9914.

Description For this test, bytes are written to the 9914 Data Out register (U622) to drive and release bus line DIO1. The state of this signal is verified at the 68302 (U626) through PB0 (BITB1). This test verifies the basic functionality of the 9914 and 75160 (U621).

High suspect components U612 and U622.

Triggers tests

Triggers are controlled by the 5064 ASIC (U618). This component has seven trigger outputs (STO1-STO7) and eight trigger inputs (STI1-STI8). Lines STI1-STI6 and STO1-STO6 are used to control the system trigger bus, line STO7 is used for Meter Complete, and line STI7 is used for External Trigger. STI8 is connected to the Group Execute Trigger signal (GET) of the 9914 IEEE-488 bus controller (U622).

Test 105.1 through 105.6 – System trigger bus

Type

Pass/Fail

Failure analysis

Defective system trigger bus.

Description

System trigger inputs are normally pulled up to 5V through the protection diodes and 5.1kΩ resistors (CR611-CR616, R648-R650 and R655-R657). The Model 2001 can generate a trigger on any of the six trigger bus inputs by turning on the appropriate FET (Q602-Q607). These FETs are controlled by system trigger outputs (STO1-STO6) of the 5064 ASIC (U618).

In test 105.1, STI1 is set up as the trigger input. The trigger 1 FET (Q606) is then turned on and off through STO1, and it is verified that this trips the trigger circuitry in the ASIC. This test is then repeated for trigger 2 through 6 for tests 105.2 through 105.6. Success indicates proper operation of the trigger bus.

High suspect components

ASIC, FETs, diodes and 5.1kΩ resistors.

Test 105.7 – External Trigger/Meter Complete

Type

Pass/Fail

Failure analysis

Short between External Trigger and Meter Complete

Description

This test is similar to System Trigger tests 105.1 through 105.6 except that there is no internal connection between External Trigger and Meter Complete. Consequently, the meaning of a failure is reversed from that of the previous trigger tests. A failure is registered if a trigger does occur. A failure indicates that a short exists between External Trigger and Meter Complete.

An alternate way to test these triggers is to externally connect a BNC cable from External Trigger to Meter Complete. When test 105.7 is run, the short should cause the test to fail. If it does not, a problem in the signal path exists.

Test 105.8 – Group Execute Trigger (GET)

Type Pass/Fail

Failure analysis GET signal not detected.

Description Trigger 8 (STI8) is set up as an input and the 9914 (U622) is then programmed to generate a GET signal.

High suspect components U618 and U622.

Test 105.11 through 105.18 – Trigger shorts

Type Pass/Fail

Failure analysis Short detected between system triggers.

Description In test 105.11, STI1 is programmed as the trigger input. Each of the other triggers (STI2 through STI7 and GET) are programmed to toggle in sequence. If a trigger is detected at STI1, a short is indicated and the test fails. The test is repeated for STI2 through STI8 in tests 105.12 through 105.18.

Ordinarily, Built-In-Tests should be run with no external connections. However, the Trigger Shorts tests may be used to verify proper operation at the external trigger bus connector (J1029, J1030). For example, by shorting pins 1 and 2, tests 105.11 and 105.12 should fail indicating that the short was detected between system trigger 1 and system trigger 2.

A/D converter and analog circuitry tests

There are three data words used to configure and control the instrument. The DC STB data word is used to control A/D multiplexing and the input gain configuration. The R1 STB data word is used to control the DCV and ohms configuration. The R2 STB data word is used to control the ACV configuration. Each 32-bit data word is generated in the digital section and is passed by U808 to the three sets of control shift registers. U808 uses the two least significant bits of a data word to determine which strobe (DC_STB, R1_STB or R2_STB) will be active to latch the data word into the appropriate shift registers.

Tables 2-5 through 2-7 lists the control registers for the three strobes and provides a functional description of each bit. The documentation for each of the following Built-In Tests includes the logic states for the registers after each test is manually run. Also included as a troubleshooting aid is Table 2-8 which provides the state of the control lines for each selected input of multiplexer U511.

Test 200.1 – A/D zero

Type

Pass/Fail

Failure analysis

No A/D communication and/or noisy A/D.

Description

This test turns on Q328 by setting /HIV low and turns on Q525 by setting /DIVIDER low. Switches U319 (/ZERO pulled low) and U318 (/X1 pulled low) are closed and U808 is set for line cycle integration.

Common (ZERO) zeroes the A/D buffer (x1 gain). The zero is then applied to the A/D converter. The A/D is triggered until the Charge Balance (CB) counts are the same. The value is then stored and compared to a zero-by-design CB value. Final Slope (FS) counts are also stored. If the A/D cannot make this measurement, the test will fail.

High suspect components

U808 (not communicating with the digital section) and most any component in A/D circuitry.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 200.2 – A/D noise

Type

Pass/Fail

Failure analysis

Noisy signal conditioning.

Description

This test uses the same circuit setup as test 200.1. The A/D is triggered for 10 readings and a mininmum/maximum comparison is done for 30 counts or less. Failing this test indicates A/D buffer noise or A/D converter circuit noise.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 200.3 – FAST circuit

Type

Pass/Fail

Failure analysis

Defective FAST circuit

Description

This test uses the same circuit setup as Test 200.1. Line cycle integration and FAST is selected on U808. The FAST circuit includes U806 (FS1), Q813, R842, and the FS1 control line from U808.

High suspect components

U606, Q813, R842 and U808

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	1	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 200.4 – x10 line cycle integration

Type

Pass/Fail

Failure analysis

Cannot select x10 line cycle integration.

Description

Same circuit setup as test 200.1 but x10 line cycle integration selected. Configures I3 through I13 for x10 line integration.

High suspect components

U801, U800, and U808.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 0		Q7: 1		Q7: 0
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 1		Q3: 1		Q3: 0
	Q4: 1		Q4: 0		Q4: 1
	Q5: 1		Q5: 0		Q5: 1
	Q6: 0		Q6: 0		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 0
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 0		Q7: 1		Q7: 0
	Q8: 0		Q8: 0		Q8: 1
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 1				Q4: 1
	Q5: 1				Q5: 1
	Q6: 1				Q6: 1
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 200.5 – x0.1 line cycle integration

Type

Pass/Fail

Failure analysis

Cannot select x0.1 line cycle integration.

Description

Same circuit setup as test 200.1 but x0.1 line cycle integration selected. Configures I3 through I13 for x0.1 line integration.

High suspect components

U801, U800, and U808.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	0		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	0	U305	Q1:	1	U500	Q1:	1
	Q2:	0		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 200.6 – x0.02 line cycle integration

Type

Pass/Fail

Failure analysis

Cannot select x0.02 line cycle integration.

Description

Same circuit setup as test 200.1 but x0.02 line cycle integration selected. Configures I3 through I13 for x0.02 line integration.

High suspect components

U801, U800, and U808.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	0		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	0	U305	Q1:	1	U500	Q1:	1
	Q2:	0		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 200.7 – x0.01 line cycle integration

Type

Pass/Fail

Failure analysis

Cannot select x0.01 line cycle integration.

Description

Same circuit setup as test 200.1 but x0.01 line cycle integration selected. Configures I3 through I13 for x0.01 line integration.

High suspect components

U801, U800, U808, and FAST circuitry (see test 200.3).

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	1	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	0		Q4:	1		Q4:	0
	Q5:	0		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	0	U305	Q1:	1	U500	Q1:	1
	Q2:	0		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 201.1 – Test cal zero

Type

Circuit exercise

Description

Same circuit setup as test 200.1. A zero reading is acquired for tests 201.2 and 201.3.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 201.2 – 7V reference

Type

Pass/Fail

Failure analysis

Cannot measure 7V at A/D IN.

Description

This test turns on Q328 by setting /HIV low and turns on Q525 by setting /DIVIDER low. Switches U317 (/REF pulled low) and U318 (/X1 pulled low) are closed and U808 is set for line cycle integration.

REF OUT (7V) is connected to the A/D buffer at x1 gain and is then applied to the A/D converter. The A/D is triggered and the REF OUT counts are stored and compared to a design REF OUT value.

High suspect components

U330, U329, U328 and associated resistors and capacitors.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	0		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 201.3 – 1.75V reference

Type

Pass/Fail

Failure analysis

Cannot measure 1.75V at A/D IN.

Description

This test turns on Q328 by setting /HIV low and turns on Q525 by setting /DIVIDER low. Two switches of U318 (/2VREF pulled low) and (/X1 pulled low) are closed and U808 is set to line cycle integration.

The 1.75V reference is connected to the A/D buffer at x1 gain and 1.75V REF is applied to the A/D converter. The A/D is triggered and the 1.75V REF counts are stored. A calculation is performed using the values stored in tests 200.1, 200.2, and 200.3.

High suspect components

U327, U330, U329, U328 and associated resistors and capacitors.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 1		Q6: 0
	Q7: 0		Q7: 1		Q7: 0
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 0		Q5: 1
	Q6: 0		Q6: 0		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 0
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 1		Q7: 1		Q7: 0
	Q8: 0		Q8: 0		Q8: 1
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 0				Q4: 1
	Q5: 1				Q5: 1
	Q6: 1				Q6: 1
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 300.1 – A/D mux, A/D buffer, 7V reference, x1.5 gain

Type

Pass/Fail

Failure analysis

Cannot measure 10.5V ±1.5V at A/D IN.

Description

This test switches the 7V reference (REF OUT from U329, pin 1) through analog switch U317 (/REF pulled low) to the non-inverting input of Op Amp U322. Analog switch U319 (/./2 pulled low) is closed and Q306 is turned on (BUF = 0V) connecting R327 to common. This configuration results in a gain of x1.5. Measure 10.5V (7V x 1.5) at A/D IN.

High suspect components

U317, U319, Q306, Q342, R334, R327 and R422.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	0		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 300.2 – A/D mux, A/D buffer, 1.75V reference, x5 gain

Type

Pass/Fail

Failure analysis

Cannot measure 8.75V ±0.875 at A/D IN.

Description

This test switches the 1.75V reference (U327 output) through analog switch U318 (/2VREF pulled low) to the non-inverting input of Op Amp U322. Analog switch U318 (/X5 pulled low) is closed to use resistors R326 and R335 to obtain a gain of x5. Measure 8.75V (1.75V x 5) at A/D IN.

High suspect components

U318, R326 and R335.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	0					Q2:	1
	Q3:	1					Q3:	0
	Q4:	0					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 300.3 – A/D mux, A/D buffer, 0V reference, x5 gain

Type

Pass/Fail

Failure analysis

Cannot measure 0V ±0.01V at A/D IN.

Description

This test switches common through R340 and analog switch U319 (/ZERO pulled low) to the non-inverting input of Op Amp U322. Analog switch U318 (/X50 pulled low) is closed to use thick film resistor R215 to obtain a gain of x50. The actual gain is not tested here, but the presence of R215 is detected. A later test will check the actual value. Measure 0V at A/D IN.

High suspect components

U319, U318 and R215.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	0					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 301.1 – Input buffer, front end (FE) zero

Type

Pass/Fail

Failure analysis

Cannot measure 0V ±0.02V at A/D IN.

Description

The front end (FE) zero (common) is switched through U323 (4W OHM pulled low) and Q527 (FE ZERO = 0V) to Q330. Pin 6 of Q330 and pin 6 of input buffer U335 should be at 0V. Zero is then routed through Q313 and Q308 (//1 = 0V) to the non-inverting input of Op Amp U322. Analog switch U318 (/X1 pulled low) is closed to obtain a gain of x1. Measure 0v at A/D IN.

High suspect components

U323, Q527, R200, R213, Q330, Q335, Q336, U335, Q313, Q308, R424, R423, R353, U318 and R278.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 0
	Q2: 1		Q2: 0		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 0		Q6: 0
	Q7: 0		Q7: 1		Q7: 0
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 1		Q5: 1
	Q6: 0		Q6: 1		Q6: 1
	Q7: 0		Q7: 1		Q7: 1
	Q8: 0		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 0		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 0
	Q4: 0		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 1		Q7: 1		Q7: 0
	Q8: 1		Q8: 0		Q8: 1
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 1				Q4: 1
	Q5: 1				Q5: 1
	Q6: 1				Q6: 1
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 301.2 – Input buffer, divided by 100

Type

Pass/Fail

Failure analysis

Cannot measure 0V ±0.01V at A/D IN.

Description

This test routes 0V (common) to input buffer U335. The 0V signal path to the input buffer is through FET Q328 (/HIV pulled low), the 100kΩ leg of R394, FET Q525 (/DIVIDER = 0V) and finally through signal FETs Q522 and Q523 (VLO2 is floating and pin 4 of U339 is at 0V) to pin 2 of Q330. The 0V output of the input buffer is then routed to Op Amp U322, which is configured for x1 gain. Measure 0V at A/D IN.

High suspect components

Q328, R394, Q525, Q522, Q523, U339, R201, R242 and R428.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 302.1 – Ohms; zero reference measurement for test 302.2

Type

Circuit Exercise

Description

This measurement is the same as the one in test 301.1. Although the reading is very close to 0V, it is not exactly zero due to offsets in the input buffer and A/D buffer circuits. This reading is used as the zero reference for test 302.2.

High suspect components

Q328, R394, Q525, Q522, Q523, U339, R201, R242 and R428.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	0		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 302.2 – Ohms; open circuit and protection

Type

Pass/Fail

Failure analysis

Cannot measure 5.9V ±0.59V at A/D IN.

Description

This test closes the ohms circuit feedback loop by selecting the 9.2mA ohms source resistor path (parallel combination of R355, R356 and R357). The parallel resistor combination is configured by closing the switches at pins 1 and 12 of U332. FETs Q312 and Q320 are on (/HI OHM pulled low). Measure 7V across the resistors.

There is no load connected to the ohms source circuit. Current flows through CR335, zener VR304 and resistor R375 to common. The 5.9V drop across this combination (0.6V across CR335, 5.1V across VR304, and 0.2V across R375) is routed through Q321, Q323 and K300 (OHM control line pulled low) to OHMS. From OHMS, the 5.9V is applied to the input buffer through the 9.9MΩ leg of R394 and Q525 (/DIVIDER = 5.9V). Op Amp U322 is set up for x1 gain. Measure 5.9V at A/D IN.

NOTE: This is the first test that checks any part of the ohms circuit. The components listed above are not necessarily all of the components that are tested. The ohms circuit is used for most of the 300 series tests that follow. If test 302.2 fails, then the other 300 level tests will most likely fail.

High suspect components

K300, Q323, Q321, R377, Q320, Q312, CR335, VR304, R375, U331, U332, U333, U324, Q317, U330, R355, R356 and R357.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	0		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 303.1 – Input path; zero reference measurement for test 303.2

Type

Circuit Exercise

Description

This measurement is exactly the same as test 301.1. Although the reading is very close to 0V, it is not exactly zero due to offsets in the input buffer and A/D buffer circuits. This reading is used as the zero reference for test 303.2.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 0
	Q2: 1		Q2: 0		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 0		Q6: 0
	Q7: 0		Q7: 1		Q7: 0
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 1		Q5: 1
	Q6: 0		Q6: 1		Q6: 1
	Q7: 0		Q7: 1		Q7: 1
	Q8: 0		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 0		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 0
	Q4: 0		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 1		Q7: 1		Q7: 0
	Q8: 1		Q8: 0		Q8: 1
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 1				Q4: 1
	Q5: 1				Q5: 1
	Q6: 1				Q6: 1
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 303.2 – Input path; open circuit ohms and ohms protection

Type

Pass/Fail

Failure analysis

Cannot measure 5.9V ±0.59V.

Description

This test uses the same open circuit ohms voltage as test 302.2, except the voltage is routed through the input path of Q340, Q339, Q338, Q337, and Q333 (/LOV/OHM = 5.9V)) to the input buffer. Op Amp U322 is set up for x1 gain. Measure 5.9V at A/D IN.

High suspect components

Q340, Q339, Q338, Q337, Q333, U336, U337, U338, R399, R400, R401, R398, R411, R410, R409 and R408.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 303.3 – Input path; front end (FE) zero protection

Type

Pass/Fail

Failure analysis

Cannot measure 2.5V ±2.5V at A/D IN.

Description

This test is identical to test 303.2, except that Q539 (FE ZERO = 0V) is turned on. Some current will flow through Q340, Q339, Q338, and Q337. With Q539 turned on, current will flow through CR329, VR511, VR510, Q539, and R369 to common. Op Amp U322 is set up for x1 gain. Measure 0 to 5V (typically around 3.5V) at A/D IN.

High suspect components

CR329, VR511, VR510, Q539 and R369.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 0	U505	Q1: 0
	Q2: 1		Q2: 0		Q2: 0
	Q3: 1		Q3: 1		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 0		Q6: 0
	Q7: 0		Q7: 0		Q7: 0
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 1		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 1		Q5: 1
	Q6: 0		Q6: 0		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 0
	Q4: 0		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 1		Q7: 1		Q7: 0
	Q8: 1		Q8: 0		Q8: 1
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 1				Q4: 1
	Q5: 1				Q5: 1
	Q6: 1				Q6: 1
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 304.1 – Ohms sources; zero reference measurement for tests 304.2 – 304.7

Type

Circuit Exercise

Description

This measurement is exactly the same as test 301.1. Although the reading is very close to 0V, it is not exactly zero due to offsets in the input buffer and A/D buffer circuits. This reading is used as the zero reference for tests 304.2 through 304.7.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	0		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 304.2 – Ohms sources; 0.98mA and 9.2mA

Type

Pass/Fail

Failure analysis

Cannot measure 0.78V ±0.08V at A/D IN.

Description

Switches in R358 for the 0.98mA ohms source by closing the analog switches at pins 5 and 14 of U332. The parallel combination of R355, R356 and R357 (used for the 9.2mA source during normal operation) acts as the load and is connected to common through the analog switch at pin 1 of U325. FETs Q312 and Q320 are also on. 7V will appear across R358. Op Amp U322 is set up for x1 gain. Measure 0.78v at A/D IN.

High suspect components

R355, R356, R357, R358, U322 and U325.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 0
	Q2: 1		Q2: 0		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 0		Q6: 0
	Q7: 0		Q7: 0		Q7: 0
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 1		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 1		Q5: 1
	Q6: 0		Q6: 1		Q6: 1
	Q7: 0		Q7: 1		Q7: 1
	Q8: 0		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 0
	Q4: 0		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 1		Q7: 1		Q7: 0
	Q8: 0		Q8: 0		Q8: 1
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 1				Q4: 1
	Q5: 1				Q5: 1
	Q6: 1				Q6: 1
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 304.3 – Ohms sources; 89μA and 0.98mA

Type

Pass/Fail

Failure analysis

Cannot measure 0.65V ±0.065V at A/D IN.

Description

Switches in R365 for the 89uA ohms source by closing the analog switches at pins 2 and 15 of U332. R358 (used for the 0.98mA ohms source during normal operation) acts as the load and is connected to common through the analog switch at pin 5 of U325. FETs Q312 and Q320 are also on. 7V will appear across R365. Op Amp U322 is set up for x1 gain. Measure 0.65v at A/D IN.

High suspect components

R365, U322 and U325.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 304.4 – Ohms sources; 7μA and 89μA

Type

Pass/Fail

Failure analysis

Cannot measure 0.56V ±0.056V at A/D IN.

Description

Switches in R366 for the 7uA ohms source by closing the analog switches at pins 4 and 11 of U332. R365 (used for the 89uA ohms source during normal operation) acts as the load and is connected to common through the analog switch at pin 2 of U325. FETs Q312 and Q320 are also on. 7V will appear across R366. Op Amp U322 is set up for x1 gain. Measure 0.56v at A/D IN.

High suspect components

R366, U322 and U325.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 304.5 – Ohms sources; 770nA and 7μA

Type

Pass/Fail

Failure analysis

Cannot measure 0.7V ±0.07V at A/D IN.

Description

Switches in R366 for the 7μA ohms source as in test 304.4. R394 (used for the 770nA ohms source during normal operation) acts as the load and is connected to common by turning on Q328 (/HIV pulled low). FETs Q312 and Q320 are also on. 7V will appear across R366. Op Amp U322 is set up for x1 gain. Measure 0.70V at A/D IN.

High suspect components

R394 and U322.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 304.6 – Ohms sources; 70nA and 770nA

Type

Pass/Fail

Failure analysis

Cannot measure 0.7V ±0.07V at A/D IN.

Description

Switches in R354 for the 70nA ohms source by closing the analog switches at pins 1 and 12 of U332. Q324 (HI OHM pulled low) is on while Q312 and Q320 are off. This selects R354 as the only source resistor. No other resistor is in parallel with it. The load is again R394 and is connected to common through Q328. 7V will appear across R354. Op Amp U322 is set up for x1 gain. Measure 0.70V at A/D IN.

High suspect components

R354 and Q324.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 304.7 – Ohms sources; 4.4nA and 770nA

Type

Pass/Fail

Failure analysis

Cannot measure 2.2V ±0.6V at A/D IN.

Description

This test uses the same ohms source resistor (R354) as the previous test except that analog switch U323 (/200M pulled low) is closed to configure Op Amp U324 into a divide by 16 amplifier. This reduces the voltage drop cross R354 from 7V to 0.44V (7/16 = 0.44). 4.4nA is sourced through R394 to common through Q328. Op Amp U322 is set up for x50 gain. Measure 2.2V at A/D IN.

High suspect components

U323, R350, R349 and R215.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	0					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 305.1 – Input divider; zero reference measurement for test 305.2

Type

Circuit Exercise

Description

This measurement is exactly the same as test 301.1. Although the reading is very close to 0V, it is not exactly zero due to offsets in the input buffer and A/D buffer circuits. This reading is used as the zero reference for test 305.2.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	0		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 305.2 – Input divider; divide by 100

Type

Pass/Fail

Failure analysis

Cannot measure 2.95V ±0.295V at A/D IN.

Description

Basically, this test utilizes the same open circuit ohms scheme as test 302.2. The 9.2mA ohms source is connected through R394 (10MΩ) to common via Q328. The open circuit ohms circuit clamps the voltage drop across R394 to approximately 5.9V.

FET Q525 is turned on to divide the 5.9V by 100. The resultant 59mV is then applied to the input buffer. Op Amp U322 is configured for x50 gain. Measure 2.95V (50 x 59mV) at the output of U322.

High suspect components

R394 (100 to 1 ratio).

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	0					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 306.1 – Ohms cal switch

Type

Pass/Fail

Failure analysis

Cannot measure 0V ±0.001V at A/D IN.

Description

On U325, OHM CAL is connected to common by closing the analog switches at pins 1 and 12. Analog switch U320 (/OHM CAL pulled low) routes this 0V signal to the A/D buffer. Op Amp U322 is set up for x1 gain. Measure 0V at the output of U322.

High suspect components

U320.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	0		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 307.1 – Cal divider; zero reference for test 307.2

Type

Circuit Exercise

Description

This measurement is exactly the same as test 301.1. Although the reading is very close to 0V, it is not exactly zero due to offsets in the input buffer and A/D buffer circuits. This reading is used as the zero reference for test 307.2.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	0		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 307.2 – Cal divider; A/D mux/10

Type

Pass/Fail

Failure analysis

Cannot measure 3.8V ±0.38V at A/D IN.

Description

Uses the 0.98mA ohms source and parallel combination of R355, R356 and R357 as a load (same as test 304.2). The 0.78V output of the input buffer is divided by 10 (R342 and R343) and routed through U319 (/CAL pulled low) to the A/D buffer. The 7.8 mV is applied to the non-inverting input of Op Amp U322, which is configured for x50 gain. Measure 3.8V (7.8mV x 50) at A/D IN.

High suspect components

U319, R342 and R343.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	0		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	0					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 307.3 – Cal divider; A/D mux/buffer (x-0.5)

Type

Pass/Fail

Failure analysis

Cannot measure -2.9V ±0.4V at A/D IN.

Description

Uses the 9.2mA ohms source basically the same way as test 305.2. A no load condition causes the 5.9V open circuit ohms circuit to be operational. This voltage is routed through the 9.9MΩ leg of R394 and Q525 to the non-inverting input of Op Amp U341. The unity gain amplifier provides 5.9V at its output (BSCOM).

BSCOM is routed through Q304 and U319 (//2 pulled low) to the inverting input of Op Amp U322. Analog switch U319 (/ZERO pulled low) is also closed. This configuration around U322 produces a gain of -0.5. Measure -2.9V (5.9V x -0.5) at A/D IN.

High suspect components

U341, Q304, Q341, and R421.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	0		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	0	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 308.1 – 4-digit mode; A/D MUX signal path

Type

Pass/Fail

Failure analysis

Cannot measure 0.78V ±0.078V at A/D IN.

Description

The ohms source is configured the same as in tests 304.2 and 307.2. The output of U335 is 0.78V, which is the same as bootstrap common (BSCOM). In 4-digit mode, BSCOM is routed through U319 (/4 DIGIT pulled low) to the non-inverting input of Op Amp U322, which is configured for x1 gain. Measure 0.78V at the output of U322.

High suspect components

U319 and R212.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	0		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	0		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	0		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 308.2 – 4-digit mode; A/D MUX zero path

Type

Pass/Fail

Failure analysis

Cannot measure 0V ±0.01V at A/D IN.

Description

Common for the 4-digit mode is routed through U317 (4 DIGIT pulled low) and U319 (/4 DIGIT pulled low) to the non-inverting input of Op Amp U322, which is configured for x1 gain. Measure 0V at the output of U322.

High suspect components

U317 (4 DIGIT)

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	0		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	0	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	1		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 309.1 – Amps; 200µA range

Type

Pass/Fail

Failure analysis

Cannot measure 0.089V ±0.0089V at A/D IN.

Description

The 89µA ohms source is switched through U323 (/ACAL pulled low) and the 200µA range switch U317 (/200µA pulled low). Current flows through thick film R344 (all three resistors), R592 and R591 to common. The resulting voltage drop, which applies to all of the 309 series tests, is switched by U320 (/DCA pulled low) of the A/D MUX to the non-inverting input of Op Amp U322, which is configured for x1 gain. Measure 89mV (89µA x 1000.01ohm) at A/D IN.

High suspect components

U323, U317, R344, R592, R591 and U320.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	0					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 309.2 – Amps; 2mA range

Type

Pass/Fail

Failure analysis

Cannot measure 0.098V ±0.0098V at A/D IN.

Description

The 0.98A ohms source is switched through U323 (/ACAL pulled low), U317 (/2mA pulled low), the 90Ω and 9Ω legs of R344, R592 and R591 to common. Op Amp U322 is configured for x1 gain. Measure 98mV (0.98mA × 100.01Ω) at A/D IN.

High suspect components

U317, R344, R592 and R591.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	0		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	0					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 309.3 – Amps; 20mA range

Type

Pass/Fail

Failure analysis

Cannot measure 0.092V ±0.0092V at A/D IN.

Description

The 9.2mA ohms source is switched through U323 (/ACAL pulled low), Q311, the 9Ω leg of R344, R592 and R591 to common. Op Amp U322 is configured for x1 gain. Measure 92mV (9.2mA × 10.01Ω) at A/D IN.

High suspect components

Q311, R344, R592 and R591.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	0		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	0					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 309.4 – Amps; reference measurement for tests 309.5 and 309.6

Type

Circuit Exercise

Description

The 9.2mA ohms source is applied through U323 (/ACAL pulled low) directly to the amps protection diodes CR305 and CR309. None of the amps switches or FETS are closed. This measurement determines circuit trace resistance loss between common at the ohms source and common at R591. Op Amp U322 is configured for x50 gain. Measure approximately 10 mV at A/D IN which is used as the zero reference for tests 309.5 and 309.6.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	0					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	0					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 309.5 – Amps; 200mA range

Type

Pass/Fail

Failure analysis

Cannot measure (0.475V + Test 309.4) ±0.0475V at A/D.

Description

The 9.2mA ohms source is switched through U323 (/ACAL pulled low), Q309 and Q307 (/200mA = +15v), R592 and R591 to common. Op Amp U322 is configured for x50 gain. Measure approximately 475mV at A/D IN (9.2mA × 1.01Ω × 50) + (zero reference reading from test 309.4).

High suspect components

Q309, Q307, R592 and R591.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	0		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	0					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	0					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 309.6 – Amps; 2A range

Type

Pass/Fail

Failure analysis

Cannot measure (0.0462V + Test 309.4) ±0.00462V at A/D IN.

Description

The 9.2mA ohms source is switched through U323 (/ACAL pulled low), Q310 and Q305 (/2A = +15v) and R591 to common. Op Amp U322 is configured for x50 gain. Measure approximately 46mV at A/D IN (9.2mA x 0.1Ω x 50) + (zero reference reading from test 309.4).

High suspect components

Q310, Q305 and R591.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	0		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	1				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	0					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	0					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 310.1 – Amps protection

Type

Pass/Fail

Failure analysis

Cannot measure 1.7V ±0.3V at A/D IN.

Description

The 9.2mA ohms source is set up to source current on the 200µA range as in test 309.1. The load resistance for the 200µA range is 1000.01Ω. Diodes CR305 and CR309 clamp the amps circuit voltage to three diode drops. This voltage is applied to Op Amp U322 through U320 (/DCA pulled low) in a similar manner as in the 309 series tests. Op Amp U322 is configured for x1 gain. Measure 1.7V at A/D IN.

High suspect components

CR309 and CR305.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	0		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	1					Q5:	1
	Q6:	0					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 400.1 – DAC; -4.21V output

Type

Pass/Fail

Failure analysis

DAC output not -4.21V ±0.4V.

Description

The TRIG bits for OUT B of the DAC (U531) are programmed to produce -4.21V at PRE-COM+ (pin 1 of U528). This signal is routed through R560 and U532 (DAC line pulled low). This line, now called ACF, is selected by multiplexer U511. The output (OUT) of the multiplexer is routed through buffer U342 and resistor R223 (where the line is called ACV/A). The signal on ACV/A is then routed through U320 (/AC pulled low) and applied to Op Amp U322. Measure -4.21v at A/D IN.

High suspect components

Q310, Q305 and R591.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 1
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 1		Q6: 0
	Q7: 0		Q7: 1		Q7: 0
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 0		Q5: 1
	Q6: 0		Q6: 0		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 1
	Q2: 1		Q2: 1		Q2: 1
	Q3: 1		Q3: 1		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 1
	Q6: 1		Q6: 1		Q6: 0
	Q7: 1		Q7: 1		Q7: 0
	Q8: 1		Q8: 0		Q8: 0
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 1				Q4: 1
	Q5: 0				Q5: 1
	Q6: 1				Q6: 0
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 400.2 – DAC; -2.08V output

Type Pass/Fail

Failure analysis DAC output not -2.08V ±0.34V.

Description Same as test 400.1 except OUT B of the DAC is configured for -2.08V. Measure -2.08V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 400.3 – DAC; 0V output

Type

Pass/Fail

Failure analysis

DAC output not 0.001V ±0.28V.

Description

Same as test 400.1 except OUT B of the DAC is configured for 0V. Measure 0V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 400.4 – DAC; 2.25V output

Type

Pass/Fail

Failure analysis

DAC output not 2.25V ±0.34V.

Description

Same as test 400.1 except OUT B of the DAC is configured for 2.25V. Measure 2.25V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 400.5 – DAC; 4.33V output

Type

Pass/Fail

Failure analysis

DAC output not 4.33V ±0.4V.

Description

Same as test 400.1 except OUT B of the DAC is configured for 4.33V. Measure 4.33V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 401.1 – Signal switching; zero cal switch

Type

Pass/Fail

Failure analysis

Cannot measure 0V ±0.001V at A/D IN.

Description

Common is routed to the ACF line through U526 (SHORT pulled low). ACF is then routed through multiplexer U511. The output of the multiplexer (OUT) follows the same path to the A/D buffer (U322) as the 400 series tests. U322 is configured for x1 gain. Measure 0V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 402.1 – Signal switching; frequency switch

Type

Pass/Fail

Failure analysis

Cannot measure 0.032V ±0.005V at A/D IN.

Description

OUT B of the DAC (U531) is set up to output 4.33V at PRECOMP+ (U528 pin 1). The operation of the frequency switch, U522 (FREQ pulled low), is verified by dividing the PRECOMP+ voltage by the voltage ratio across R560 and R558. The "on" resistance (approximately 25Ω) of the analog switch (U522) is added to the resistance of R558 since it is part of the ratio. Again, as in the 400 series tests, this voltage is routed to the A/D buffer (U322) which is configured for x1 gain. Measure 32mV at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	0
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 403.1 – Signal switching; ground switch

Type

Pass/Fail

Failure analysis

Cannot measure 0.001V ±0.005V at A/D IN.

Description

Common at pin 9 of U511 is multiplexed to pin 8 (OUT) and measured in the same manner as the previous 400 series tests. Measure 0V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	1
	Q4:	1					Q4:	0
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 404.1 – Absolute value (x1 gain); -full-scale DAC output

Type

Pass/Fail

Failure analysis

Cannot measure 4.21V ±0.4V at A/D IN.

Description

DAC U531 is programmed to generate -4.21 VDC at PRECOMP+. That signal is then applied to ACF through R560 and U532 (DAC line pulled low). ACF is routed to AMP IN via U526, Q516, and the AC input buffer.

AMP IN is tied to the inverting and non-inverting paths of the variable gain amplifier (VGA). NETOUT (output of U519) is routed to the Zero-Crossing Amplifier which, based on the polarity, generates the appropriate COMP- signal that is applied to comparator U507. The comparator selects the path that the AMP IN signal will follow through the VGA by closing the appropriate analog switches of U509.

The negative (inverting) AMP IN path is through R530, U515, U509, Q501, and U516 to pin 12 of the multiplexer (U511). The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal on ACV/A is switched through U320 (/AC pulled low) to the A/D buffer (U322) which is configured for x1 gain. Measure +4.21V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 404.2 – Absolute value (x1 gain); -half scale DAC output

Type

Pass/Fail

Failure analysis

Cannot measure 2.08V ±0.34V at A/D IN.

Description

ADC U531 is programmed to generate -2.08 VDC at PRECOMP+. This signal follows the same path as test 404.1. Measure +2.08V at A/D IN.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 1
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 1
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 1		Q6: 0
	Q7: 0		Q7: 1		Q7: 1
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 0		Q5: 1
	Q6: 0		Q6: 0		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 1
	Q4: 1		Q4: 1		Q4: 1
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 0
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 0		Q8: 0
U303	Q1: 0			U501	Q1: 0
	Q2: 1				Q2: 0
	Q3: 1				Q3: 1
	Q4: 1				Q4: 1
	Q5: 0				Q5: 1
	Q6: 1				Q6: 0
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 404.3 – Absolute value (x1 gain); zero DAC output

Type

Pass/Fail

Failure analysis

Cannot measure 0.001V ±0.28V at A/D IN.

Description

DAC U531 is programmed to generate +0.001 VDC at PRECOMP+. This signal follows the same path to the variable gain amplifier (VGA) as test 404.1. However, for this test AMP IN is positive. Thus, the COMP- signal applied to comparator U507 selects the non-inverting path for the AMP IN signal.

The positive (non-inverting) AMP IN path is through R530, Q509, Q507, U519, R531, U509, Q501, and U516 to pin 12 of the multiplexer (U511). The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal on ACV/A is switched through U320 (/AC pulled low) to the A/D buffer (U322) which is configured for x1 gain. Measure +0.001V at A/D IN.

High suspect components

Q310, Q305 and R591.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 404.4 – Absolute value (x1 gain); +half-scale DAC output

Type

Pass/Fail

Failure analysis

Cannot measure 2.25V ±0.34V at A/D IN.

Description

DAC U531 is programmed to generate +2.25 VDC at PRECOMP+. This signal follows the same path as test 404.3. Measure +2.25V at A/D IN.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 1
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 1
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 1		Q6: 0
	Q7: 0		Q7: 1		Q7: 1
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 0		Q5: 1
	Q6: 0		Q6: 0		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 0
	Q4: 1		Q4: 1		Q4: 1
	Q5: 1		Q5: 1		Q5: 1
	Q6: 1		Q6: 1		Q6: 1
	Q7: 1		Q7: 1		Q7: 0
	Q8: 1		Q8: 0		Q8: 1
U303	Q1: 0			U501	Q1: 0
	Q2: 1				Q2: 0
	Q3: 1				Q3: 1
	Q4: 1				Q4: 1
	Q5: 0				Q5: 1
	Q6: 1				Q6: 0
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 404.5 – Absolute value (x1 gain); +full-scale DAC output

Type

Pass/Fail

Failure analysis

Cannot measure 4.33V ±0.4V at A/D IN.

Description

DAC U531 is programmed to generate +4.33 VDC at PRECOMP+. This signal follows the same path as test 404.3. Measure +4.33V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.1 – Absolute value (x1 gain); large +DAC output

Type

Circuit Exercise

Description

DAC U531 is programmed to generate +0.51 VDC at PRECOMP+. The signal at PRECOMP+ is routed to ACF via R560 and U532 (DAC line pulled low). The signal at ACF is then switched through multiplexer U511. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain. Measure the actual voltage value at A/D IN (around +0.51V). This DAC voltage value is measured and stored. This voltage will be applied to the variable gain amplifier (VGA) that will be set for x10 gain in test 405.2. The applied value to the x10 VGA and the measured output value can be compared to check accuracy of the VGA.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	0
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.2 – Absolute value x10 gain comparison; large +DAC output

Type

Pass/Fail

Failure analysis

Voltage at A/D IN not the same as test 405.1.

Description

DAC U531 is programmed to generate +0.51 VDC at PRECOMP+. That signal is then applied to ACF through R560 and U532 (DAC line pulled low). ACF is routed to AMP IN via U526, Q516, and the AC input buffer.

AMP IN is tied to the inverting and non-inverting paths of the variable gain amplifier (VGA). NETOUT (output of U519) is routed to the Zero-Crossing Amplifier which, based on the polarity, generates the appropriate COMP- signal that is applied to comparator U507. The comparator selects the path that the AMP IN signal will follow through the VGA by closing the appropriate analog switches of U509.

The positive (non-inverting) AMP IN signal path with the VGA at x10 is through R530, Q508, Q507, U519, R531, U509, Q501, and U516 to pin 12 of multiplexer U511. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain.

Measure the voltage at A/D IN. It should be same value that was measured in test 405.1.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.3 – Absolute value x10 gain comparison; small +DAC Output

Type

Circuit Exercise

Description

This test is the same as test 405.1 except that DAC U531 is programmed to generate +0.190 VDC at PRECOMP+. As in test 405.1, measure the actual voltage value at A/D IN (around +0.190V) and compare it to the measurement in the next test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	0
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.4 – Absolute value x10 gain comparison; small +DAC output

Type

Pass/Fail

Failure analysis

Voltages at A/D IN not the same as test 405.3.

Description

This test is the same as test 405.2 except that DAC U531 is programmed to generate +0.190 VDC at PRECOMP+. As in test 405.1, measure the voltage at A/D IN. It should be same value that was measured in test 405.3.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.5 – Absolute value x10 gain comparison; small –DAC output

Type

Circuit Exercise

Description

This test is the same as test 405.1 except that DAC U531 and Op Amp pair U528 are set up to generate -0.210 VDC at PRECOMP+. As in test 405.1, measure the actual voltage value at A/D IN (around -0.210V) and compare it to the measurement in the next test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	0
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.6 – Absolute value x10 gain comparison; small –DAC output

Type

Pass/Fail

Failure analysis

Voltage at A/D IN not the same as test 405.5.

Description

DAC U531 is programmed to generate -0.210 VDC at PRECOMP+. This signal follows the same path to the variable gain amplifier (VGA) as test 405.2. However, since AMP IN is negative, comparator U507 will select the inverting path for the AMP IN signal.

The negative (inverting) AMP IN signal path with the VGA at x10 is through R530, U515, U509, Q501, and U516 to pin 12 of multiplexer U511. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain.

Measure the voltage at A/D IN. It should be same value that was measured in test 405.5.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.7 – Absolute value x10 gain comparison; large –DAC output

Type

Circuit Exercise

Description

This test is the same as test 405.1 except that DAC U531 is programmed to generate -0.490 VDC at PRECOMP+. As in test 405.1, measure the actual voltage value at A/D IN (around -0.490V) and compare it to the measurement in the next test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	0
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 405.8 – Absolute value x10 gain comparison; large –DAC output

Type

Pass/Fail

Failure analysis

Voltage a A/D IN not the same as test 405.7.

Description

This test is the same as test 405.6 except that DAC U531 is programmed to generate -0.490 VDC at PRECOMP+. As in test 405.6, measure the voltage at A/D IN. It should be same value that was measured in test 405.7.

High suspect components

Q310, Q305 and R591.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 406.1 – Test buffer; measure DAC output for test 406.6

Type

Circuit Exercise

Description

DAC U531 is programmed to provide -1.13 VDC at PRECOMP+. The signal at PRECOMP+ is routed to ACF via R560 and U532 (DAC line pulled low). The signal at ACF is then switched through multiplexer U511. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain.

Measure the actual voltage value at A/D IN (around -1.13V). This DAC voltage value is measured and stored. This voltage will be used in tests 406.2 and 406.3. In test 406.6, circuit accuracy is checked by comparing the applied voltage value to the measured output (SELFTEST OUT) value.

Bit pattern

DC_STB Registers		R1_STB Registers		R2_STB Registers	
U801	Q1: 0	U307	Q1: 1	U505	Q1: 1
	Q2: 1		Q2: 1		Q2: 1
	Q3: 1		Q3: 0		Q3: 1
	Q4: 1		Q4: 1		Q4: 1
	Q5: 1		Q5: 1		Q5: 0
	Q6: 0		Q6: 1		Q6: 0
	Q7: 0		Q7: 1		Q7: 1
	Q8: 0		Q8: 1		Q8: 0
U800	Q1: 1	U305	Q1: 1	U500	Q1: 1
	Q2: 1		Q2: 0		Q2: 1
	Q3: 0		Q3: 1		Q3: 0
	Q4: 0		Q4: 0		Q4: 1
	Q5: 0		Q5: 0		Q5: 1
	Q6: 0		Q6: 0		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 1		Q8: 1
U300	Q1: 1	U302	Q1: 1	U530	Q1: 0
	Q2: 1		Q2: 1		Q2: 0
	Q3: 1		Q3: 1		Q3: 1
	Q4: 1		Q4: 1		Q4: 0
	Q5: 1		Q5: 1		Q5: 0
	Q6: 1		Q6: 1		Q6: 1
	Q7: 1		Q7: 1		Q7: 1
	Q8: 1		Q8: 0		Q8: 0
U303	Q1: 0			U501	Q1: 1
	Q2: 1				Q2: 1
	Q3: 1				Q3: 0
	Q4: 1				Q4: 1
	Q5: 0				Q5: 1
	Q6: 1				Q6: 0
	Q7: X				Q7: X
	Q8: X				Q8: X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 406.2 – Test buffer output (-1.13V)

Type

Circuit Exercise

Description

DAC U531 is programmed to generate -1.13 VDC at PRECOMP+. The signal at PRECOMP+ is routed to ACF via R560 and U532 (DAC line pulled low). ACF is routed to AMP IN through U526, Q516, and the AC input buffer. The signal at AMP IN is routed through U522 (SELFTEST1 pulled low) and then applied to the inverting x5 gain amplifier (U523, R542 and R533).

The amplified and inverted AMP IN voltage from U523 is stored in C529 and applied to buffer Q505. The voltage value at SELFTEST OUT is the sum of the voltage on C529 and the V_{GS} drop across Q505. The signal on SELFTEST OUT is then applied to pin 11 of multiplexer U511. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain. Measure the voltage at A/D IN. The computed voltage level at A/D IN is as follows:

$V_{A/D\ IN} = |(A \times 4.8446)+B|$ where; A is measured value from test 406.1

B is the V_{GS} drop across Q505

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 406.3 – Read test buffer for test 406.6

Type

Circuit Exercise

Description

Same as test 406.2 except the value is read and stored for use for the comparison calculation in test 406.6.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 406.4 – Test buffer; read DAC output for test 406.6

Type

Circuit Exercise

Description

This test is the same as test 406.1 except that DAC U531 is programmed to generate -0.01 VDC at PRECOMP+.

Measure the actual voltage value at A/D IN (around -0.01V). This DAC voltage value is measured and stored. This voltage will be used in tests 406.5 and 406.6.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 406.5 – Test buffer output (-0.01V)

Type

Circuit Exercise

Description

This test is the same as test 406.2 except that DAC U531 is programmed to generate -0.01 VDC at PRECOMP+.

Measure the voltage at A/D IN. The computed voltage level at A/D IN is as follows:

$V_{A/D\ IN} = |(A \times 4.8446) + B|$

where; A is measured value from test 406.4
B is the V_{GS} drop across Q505

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 406.6 – Voltage comparison

Type

Pass/Fail

Failure analysis

Voltage comparison is not less than 500mV.

Description

Same as test 406.5 except the value is stored and used for the comparison calculation in this test. The measurement compares the DAC voltages to the test buffer voltages. The comparison is calculated as follows:

$$|[(V_{TEST406.1} - V_{TEST406.4}) \times 4.8446] - (V_{TEST406.3} - V_{TEST406.6})|$$

The absolute value of the difference should be less than 500mV.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	1
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	0
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 407.1 – Front end; 2V range

Type

Pass/Fail

Failure analysis

Cannot measure 7V ±0.15V at A/D IN.

Description

The signal at BUFF is routed through R233, K503, K500, the input protection circuit and Q513 to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to the variable gain amplifier (VGA) and, being positive, follows the non-inverting x1 path that consists of R530, Q509, Q507, U519, R531, U509, Q501, and U516 to pin 12 of multiplexer U511.

The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	1
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	0
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	0
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 407.2 – Front end; 200V range

Type

Pass/Fail

Failure analysis

Cannot measure 0.7V ±0.2V at A/D IN.

Description

VRIN is buffered by U517 and tied to BUFF. The signal at BUFF is routed through R233 to pin 1 of NET1 (R557). The voltage at pin 4 of NET1 is routed through U526 (DCF pulled low) and Q516, and applied to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to the variable gain amplifier (VGA) and, being positive, follows the non-inverting x10 path that consists of R530, Q508, Q507, U519, R531, U509, Q501, and U516 to pin 12 of multiplexer U511.

The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	0
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 407.3 – Front end; 750V range

Type

Pass/Fail

Failure analysis

Cannot measure 0.14V ±0.04V at A/D IN.

Description

VRIN is buffered by U517 and tied to BUFF. The signal at BUFF is routed through R233 to pin 1 of NET1 (R557). The voltage at pin 4 of NET1 is routed through U526 (DCF pulled low) and Q516, and applied to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to the variable gain amplifier (VGA) and, being positive, follows the non-inverting x10 path that consists of R530, Q508, Q507, U519, R531, U509, Q501, and U516 to pin 12 of multiplexer U511.

The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	1
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	0
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 408.1 – ÷200 correction factor; circuit setup for test 408.2

Type

Circuit Exercise

Description

The DAC (U531) is programmed with "1s" and OUT A is routed to C554. The signal at BUFF is routed through R233 and applied to NET1 (R557). The signal at pin 4 of NET1 is routed through U526 (DCF pulled low) and Q516, and applied to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to Q510 via U522 (SELFTEST1 pull low) and the x5 inverting amplifier (U523, R542 and R533).

The actions of this test set up the conditions for the next test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 408.2 – ÷200 correction factor; signal stored for test 408.3

Type

Circuit Exercise

Description

The SELFTEST control line turns on Q518 driving pin 4 of NET1 (R557) to ground. At the same time, the SELFTEST control line and multivibrator U503 generates a pulse that turns on Q510 allowing the signal to be stored on C529. No measurement is made during this test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 408.3 – ÷200 correction factor; setup for test 408.5 and A/D measurement for test 408.6

Type

Circuit Exercise

Description

The DAC (U531) is programmed with "0s" (full compensation) and OUT A is routed to C554. The signal at BUFF is routed through R233 and applied to NET1 (R557). The voltage at pin 4 of NET1 is routed through U526 (DCF pulled low) and Q516, and applied to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to Q510 via U522 (SELFTEST1 pull low) and the x5 inverting amplifier (U523, R542 and R533).

The voltage on C529 is buffered by Q505 and tied to SELFTEST OUT. The signal at SELFTEST OUT is then switched through multiplexer U511. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain.

Measure the output at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 408.4 – ÷200 correction factor

Type

Circuit Exercise

Description

Same as Test 408.3, but no measurement taken.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 408.5 – ÷200 correction factor; signal stored for test 408.6

Type

Circuit Exercise

Description

The SELFTEST control line turns on Q518 driving the pin 4 of NET1 (R557) to ground. At the same time, the SELFTEST control line and multivibrator U503 generates a pulse that turns on Q510 allowing the signal to be stored on C529. No measurement is made during this test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 408.6 – ÷200 correction factor; signal comparisons

Type

Pass/Fail

Failure analysis

The measurement in step 408.3 is not less than the measurement in step 408.6.

Description

Same as test 408.2. Measure the output at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 409.1 – ÷750 correction factor; circuit setup for test 409.2

Type

Circuit Exercise

Description

The DAC (U531) is programmed with "1s" and OUT A is routed to C556. The signal at BUFF is routed through R233 and applied to NET1 (R557). The signal at pin 4 of NET1 is routed through U526 (DCF pulled low) and Q516, and applied to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to Q510 via U522 (SELFTEST1 pull low) and the x5 inverting amplifier (U523, R542 and R533).

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 409.2 – ÷750 correction factor; signal stored for test 409.3

Type

Circuit Exercise

Description

The SELFTEST control line turns on Q518 driving the signal on pin 4 of NET1 (R557) to ground. At the same time, the SELFTEST control line and multivibrator U503 generates a pulse that turns on Q510 allowing the signal to be stored on C529. No measurement is made during this test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	1
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	1
	Q6:	1		Q6:	1		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 409.3 – ÷750 correction factor; setup for test 409.5 and A/D measurement for test 409.6

Type

Circuit Exercise

Description

The DAC (U531) is programmed with "0s" and OUT A is routed to C556. The rest of this test is the same as test 408.3.

Measure the output at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 409.4 – ÷750 correction factor

Type

Circuit Exercise

Description

Same as test 408.3 but no measurement taken.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 409.5 – ÷750 correction factor; signal stored for test 409.6

Type

Circuit Exercise

Description

The SELFTEST control line turns on Q518 driving pin 4 of NET1 (R557) to ground. At the same time, the SELFTEST control line and multivibrator U503 generates a pulse that turns on Q510 allowing the signal to be stored on C529. No measurement is made during this test.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 409.6 – ÷750 correction factor; signal comparisons

Type

Pass/Fail

Failure analysis

The measurement in step 409.3 is not less than the measurement is step 409.6.

Description

Same as test 409.2. Measure the output at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	1
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	0
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	0
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 410.1 – True RMS converter

Type

Pass/Fail

Failure analysis

Cannot measure 7V ±0.18V at A/D IN.

Description

VRIN is buffered by U517 and tied to BUFF. The signal at BUFF is routed through R233, K503, K500, the input protection circuit and Q513 to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to the variable gain amplifier (VGA) and, being positive, follows the non-inverting x1 path that consists of R530, Q509, Q507, U519, R531, U509, Q501, and U516 to pin 15 of the TRMS converter U517.

The output of the U517 is routed to the multiplexer U511 through R219. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain. Measure the output at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	1
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	0
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	1
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 411.1 – Filter; true RMS

Type

Pass/Fail

Failure analysis

Cannot measure 7V ±0.18V at A/D IN.

Description

VRIN is buffered by U517 and tied to BUFF. The signal at BUFF is routed through R233, K503, K500, the input protection circuit and Q513 to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to the variable gain amplifier (VGA) and, being positive, follows the non-inverting x1 path that consists of R530, Q509, Q507, U519, R531, U509, Q501, and U516 to pin 15 of the TRMS converter U517.

The output of the U517 is routed through analog switch U510 to the filter that consists of components R220, R221, R222, C581, C582, C583, and U523. The output of the filter is connected to the multiplexer (U511) at pin 5. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain. Measure the output at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	1
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	0
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 411.2 – Filter; variable gain amplifier

Type

Pass/Fail

Failure analysis

Cannot measure 7V ±0.16V at A/D IN.

Description

VRIN is buffered by U517 and tied to BUFF. The signal at BUFF is routed through R233, K503, K500, the input protection circuit and Q513 to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to the variable gain amplifier (VGA) and, being positive, follows the non-inverting x1 path that consists of R530, Q509, Q507, U519, R531, U509, Q501, and U516 through analog switch U532 (RMS pulled low) to the filter. The filter consists of components R220, R221, R222, C581, C582, C583, and U523.

The output of the filter is connected to the multiplexer (U511) at pin 5. The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain. Measure the output at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	1	U505	Q1:	0
	Q2:	1		Q2:	1		Q2:	1
	Q3:	1		Q3:	0		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	1		Q6:	1
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	1
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	0
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	0		Q5:	1
	Q6:	0		Q6:	0		Q6:	1
	Q7:	1		Q7:	1		Q7:	1
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	1	U530	Q1:	0
	Q2:	1		Q2:	1		Q2:	0
	Q3:	1		Q3:	1		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	1
U303	Q1:	0				U501	Q1:	1
	Q2:	1					Q2:	0
	Q3:	1					Q3:	0
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	0
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

Test 412.1 – AC amps switch

Type

Pass/Fail

Failure analysis

Cannot measure 1.7V ±0.3V at A/D IN.

Description

The 9.2mA ohms source is turned on to dump current through switch U323 (ACAL pulled low) to the amps protection diodes (CR305 and CR309). The three diode voltage drop is routed through U317 (/200uA pulled low), U320 (/ACA pulled low), U510 (REL3 pulled low), U526 and Q516 to the input buffer (Q512 and U520). The buffered signal is tied to AMP IN.

The signal at AMP IN is then routed to the variable gain amplifier (VGA) and, being positive, follows the non-inverting x1 path that consists of R530, Q509, Q507, U519, R531, U509, Q501, and U516 to pin 12 of multiplexer U511.

The output (OUT) of the multiplexer is routed through buffer U342 to ACV/A. The signal at ACV/A is routed through U320 (/AC pulled low) and applied to the A/D buffer (U322), which is configured for x1 gain. Measure 1.7V at A/D IN.

Bit pattern

DC_STB Registers			R1_STB Registers			R2_STB Registers		
U801	Q1:	0	U307	Q1:	0	U505	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	1		Q3:	1		Q3:	1
	Q4:	1		Q4:	1		Q4:	1
	Q5:	1		Q5:	1		Q5:	0
	Q6:	0		Q6:	0		Q6:	0
	Q7:	0		Q7:	1		Q7:	0
	Q8:	0		Q8:	1		Q8:	0
U800	Q1:	1	U305	Q1:	1	U500	Q1:	1
	Q2:	1		Q2:	0		Q2:	1
	Q3:	0		Q3:	1		Q3:	0
	Q4:	0		Q4:	0		Q4:	1
	Q5:	0		Q5:	1		Q5:	1
	Q6:	0		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	1		Q8:	1
U300	Q1:	1	U302	Q1:	0	U530	Q1:	1
	Q2:	1		Q2:	0		Q2:	0
	Q3:	1		Q3:	0		Q3:	0
	Q4:	1		Q4:	1		Q4:	0
	Q5:	1		Q5:	1		Q5:	0
	Q6:	1		Q6:	1		Q6:	0
	Q7:	1		Q7:	1		Q7:	0
	Q8:	1		Q8:	0		Q8:	0
U303	Q1:	0				U501	Q1:	0
	Q2:	1					Q2:	0
	Q3:	1					Q3:	1
	Q4:	1					Q4:	1
	Q5:	0					Q5:	1
	Q6:	1					Q6:	1
	Q7:	X					Q7:	X
	Q8:	X					Q8:	X

Note: Tables 2-10 through 2-12 provide functional descriptions of the register bits.

3
Disassembly

3.1 Introduction

The information in this section explains how to disassemble the Model 2001. Also discussed are handling and cleaning considerations as well as the procedure to change the main CPU firmware in the event of an upgrade. This section is organized as follows:

3.2 **Handling and cleaning precautions** — Covers general precautions to take when troubleshooting inside the unit, and cleaning procedures when replacing parts.

3.3 **Static-sensitive devices** — Explains handling procedures for static-sensitive devices.

3.4 **Case cover and shield removal** — Explains how to remove the case cover. Also covered is the removal of the top shield of the analog board to allow access to analog circuitry for troubleshooting.

3.5 **PC-board removal** — Provides the procedures for removing the digital board, A/D converter board and the analog board.

3.6 **Front panel disassembly** — Explains how to remove the display board and/or the front panel switch pad.

3.7 **Cooling fan removal** — Explains how to remove the cooling fan from the chassis.

3.8 **Firmware replacement** — Provides the procedure to change firmware.

3.9 **Instrument re-assembly** — Provides some general guidelines to follow when re-assembling the Model 2001.

3.10 **Assembly drawings** — Provides mechanical drawings to assist in the disassembly and re-assembly of the Model 2001.

3.2 Handling and cleaning precautions

When servicing the instrument, care should be taken not to indiscriminately touch PC board traces to avoid contaminating them with body oils or other foreign matter. Mother board areas covered by the shield have high impedance devices or sensitive circuitry where contamination could cause degraded performance.

3.2.1 PC-board handling

Observe the following precautions when handling PC-boards:

- Wear clean cotton gloves.
- Handle PC-boards only by the edges and shields.
- Do not touch any board traces or components not associated with the repair.
- Do not touch areas adjacent to electrical contacts.

- Use dry nitrogen gas to clean dust off PC-boards.

3.2.2 Solder repairs

Observe the following precautions when it is necessary to use solder on a circuit board:

- Use an OA-based (organic activated) flux, and take care not to spread the flux to other areas of the circuit board.
- Remove the flux from the work areas when the repair has been completed. Use pure water along with clean foam-tipped swabs or a clean soft brush to remove the flux.
- Once the flux has been removed, swab only the repaired area with methanol, then blow dry the board with dry nitrogen gas.
- After cleaning, the board should be allowed to dry in a 50°C low-humidity environment for several hours.

3.3 Special handling of static sensitive devices

CMOS devices operate at very high impedance levels for low power consumption. As a result, any static that builds up on your person or clothing may be sufficient to destroy these devices, if they are not handled properly. Use the following precautions to avoid damaging them:

CAUTION

Many CMOS devices are installed in the Model 2001. In general, it is recommended that all semiconductor devices be handled as static-sensitive.

1. ICs should be transported and handled only in containers specially designed to prevent static build-up. Typically, these parts will be received in anti-static containers of plastic or foam. Keep these devices in their original containers until ready for installation.
2. Remove the devices from their protective containers only at a properly grounded work station. Also, ground yourself with a suitable wrist strap.
3. Handle the devices only by the body; do not touch the pins.
4. Any printed circuit board into which the device is to be inserted must also be grounded to the bench or table.
5. Use only anti-static type solder sucker.
6. Use only grounded tip solder irons.
7. Once the device is installed in the PC board, it is normally adequately protected, and normal handling can resume.

3.4 Case cover and shield removal

If it is necessary to troubleshoot the instrument or to replace a component, use the following procedures as required. The first procedure removes the case cover, and the second procedure removes the top shield of the analog board allowing access to analog circuitry.

3.4.1 Case cover removal

WARNING

Before removing the case cover, disconnect the line cord and any test leads from the instrument.

To remove the case cover, refer to drawing 2001-054 and perform the following steps:

1. **Remove Handle** — The handle serves as an adjustable tilt-bail. Its position is adjusted by gently pulling it away from the sides of the instrument case and swinging it up or down. To remove the handle, swing the handle below the bottom surface of the case and back until the orientation arrows on the handles line up with the orientation arrows on the mounting ears. With the arrows lined up, pull the ends of the handle out of the case.
2. **Remove Mounting Ears** — Each mounting ear is secured to the chassis with a single screw. Remove the two screws and pull down and out on each mounting ear. Note: When re-installing the mounting ears, make sure to mount the right ear to the right side of the chassis, and the left ear to the left

side of the chassis. Each ear is marked "RIGHT" or "LEFT" on its inside surface.

3. **Remove Rear Bezel** — The rear bezel is secured to the chassis by two captive screws. To remove the rear bezel, loosen the two screws and pull the bezel away from the case.
4. **Remove Grounding Screw** — Remove the grounding screw for the case cover. This screw is located on the bottom side of the instrument at the rear.
5. **Remove Chassis** — Grasp the front bezel of the instrument and carefully slide the chassis forward, out of the metal case.

The internal pc-board assemblies are now accessible.

3.4.2 Analog board top shield removal

Most of the analog circuitry is located under the top shield for the analog board. The top shield (shown in drawing 2001-050) is secured to the analog board by a single screw. To remove the top shield, simply loosen the screw and carefully lift the shield out of the chassis.

3.5 PC-boards removal

There are three pc-boards mounted in the chassis; the digital board, the A/D converter board and the analog board. The removal of these three boards are covered in this paragraph. The display board is mounted in the front panel assembly. The removal of the display board is covered in paragraph 3.6.

Any pc-board can be removed without having to remove any of the other boards. Note that the A/D converter board plugs into the analog board and can be left installed when removing the analog board.

NOTE

Before performing any of the following procedures to remove a pc-board, remove the case cover as explained in paragraph 3.4.1.

3.5.1 Digital board

The digital board is removed through the bottom of the chassis (see drawing 2001-053). Note that the power switch pushrod does not have to be removed in order to remove the digital board.

Perform the following steps to remove the digital board:

1. Unplug Cables — Turn the chassis upside-down and unplug the following cables from the digital board:
   A. Unplug the display board ribbon cable from connector J1033.
   B. Unplug the transformer cable from connector J1032.
   C. Unplug the analog board ribbon cable from connector J1027. This cable connection is located under the power switch pushrod.
   D. Unplug the fan cable from connector J1037. This two conductor cable connection is located at the rear of the digital board in front of the IEEE connector.
2. Unfasten PC-Board — Remove the following screws and nuts to unfasten the digital board from the chassis:
   A. At the rear panel, remove the two nuts that secure the IEEE connector to the chassis.
   B. Remove the screw that connects ground of the +5V regulator (U629) to the chassis. The regulator is located at the front of the digital board behind the large electrolytic capacitor (C611).
   C. Remove the four screws that secure the digital board to the chassis. One screw is located at the rear of the digital board in front of the bank of 12 capacitors. Another screw is located next to the +5V regulator (U629). The other two screws are located near the connector for the scanner card.
3. Remove Digital Board — The board is held in place by edge guides on each side. Slide the digital board forward until the board edges clear the guides, and then carefully pull the board out of the chassis.

3.5.2 A/D converter board

The A/D converter board is located under the analog board top shield (see drawing 2001-050).

Perform the following steps to remove the A/D converter board:

1. Remove Analog Top Shield — Position the chassis right-side-up. The top shield is secured to the analog board by a single screw. To remove the top shield, simply loosen the screw and carefully lift the shield out of the chassis.
2. Remove A/D Converter Board — The A/D converter board is located near the front of the instrument and is plugged into the analog board at connector J1026. The board rests on three standoffs. Each standoff has a retaining clip to hold the board securely in place. Gently pull each retaining clip away and lift the board up until it clears the clip. With the board clear of the three retaining clips, unplug the board and pull it out of the chassis.

3.5.3 Analog board

The analog board is removed through the top of the chassis (see drawing 2001-051). Perform the following steps to remove the analog board:

1. Remove Analog Top Shield — The top shield is secured to the analog board by a single screw. To remove the top shield, simply loosen the screw and carefully lift the shield out of the chassis.
2. Remove Pushrods — Remove the pushrods for the INPUTS switch and the POWER switch as follows:
   A. Using suitable pliers, grasp the INPUTS pushrod near the switch and pull forward until it disengages from the switch shaft. Remove the pushrod from the chassis.
   B. Turn the chassis upside-down. Grasp the rear end of the POWER pushrod and pull upward until it disengages from the switch shaft. Remove the pushrod from the chassis.
   C. Return the chassis to the up-right position.
3. Remove Power Transformer — Remove the power transformer (see drawing 2001-052) as follows:
   A. Disconnect the transformer ground. A kep nut is used to connect this green ground wire to a threaded stud on the chassis.
   B. Unplug the transformer. There are three plugs for the transformer. Two are located on the analog board at connectors J1024 and J1025, and the third is located on the digital board at connector J1032. Turn the chassis upside-down to gain access to the plug on the digital board. When finished, return the chassis to the up-right position.
   C. The transformer is secured to the side of the chassis by a single screw. Remove this screw and pull the transformer out of the chassis.
4. Remove AC Power Receptacle — Remove the AC power receptacle as follows:
   A. Disconnect the receptacle ground wire. A kep nut is used to connect this green ground wire to a threaded stud on the chassis.
   B. Unplug the AC power receptacle cable. The connector for this cable is located on the analog board next to the power receptacle.
   C. A spring clip on each side of the receptacle is used to secure it to the rear panel of the chassis. Press both clips inward and, at the same time, push the receptacle out of the access hole in the rear panel of the chassis.
5. Unplug Cable to Digital Board — On the left side of the analog board there is a ribbon cable going to the digital board. Turn the chassis upside-down and unplug this cable at connector J1027 on the digital board. Return the chassis to the right-side-up position.
6. Disconnect Input Terminals — There are 10 input terminal connections (five for the front and five for the rear). Nine of these terminal wires are disconnected by simply pulling them off the pin connector on the input terminals. The front panel AMPS terminal wire must be unsoldered from the analog board. The solder connection for this white/blue wire is located next to the INPUTS switch.

   Terminal wire color identification for re-assembly is provided as follows:

	Front	Rear
INPUT HI	Red	White/Red
INPUT LO	Black	White/Black
SENSE HI	Yellow	White/Yellow
SENSE LO	Grey	White/Grey
AMPS	White	White/Blue

7. Remove Regulator Clip — A metal clip is used to transfer heat from two power supply devices (R101 and Q528) to the chassis. The clip is located on the left side of the chassis towards the rear. The clip is removed by pulling it upward. You may need to use a small flat-bladed screwdriver to pry it up.

CAUTION

The regulator clip allows the chassis to serve as a heat sink for R101 and Q528. To prevent damage to these devices (due to overheating), do not fail to install the clip when re-assembling the Model 2001.

8. Unfasten Analog Board — The analog board is secured to the chassis at the rear panel by the two BNC connectors (External Trigger and Meter Complete). At the rear panel, remove the nuts and lock washers for the BNC connectors.
9. Remove Analog Board — The board is held in place by edge guides on each side of the chassis. Slide the analog board forward until the board edges clear the guides, and then carefully lift the board out of the chassis. The bottom shield on the analog board can be removed by simply pulling it off the board.

NOTE

With the analog board removed, the cooling fan can removed as explained in paragraph 3.7.

3.6 Front panel disassembly

Use the following disassembly procedure to remove the display board and/or the pushbutton switch pad. Drawing 2001-052 shows how the front panel separates from the chassis, and drawing 2001-040 shows an exploded view of the front panel assembly.

NOTE

Before performing the following procedure to remove and disassemble the front panel, remove the case cover as explained in paragraph 3.4.1.

Perform the following steps to remove and disassemble the front panel:

1. Unplug Display Cable — Turn the chassis upside-down and unplug the display cable from the digital board at connector J1033.
2. Remove Front Panel Assembly — The front panel assembly has four retaining clips that snap onto the chassis over four pem nut studs. Two retaining clips are located on each side of the front panel. Pull the retaining clips outward and, at the same time, pull the front panel assembly forward until it separates from the chassis.
3. Remove Display Board — The display board is held in place by a pc board stop. This is simply a plastic bar that runs along the bottom edge of the display board. Using a thin bladed screw driver, pry the plastic bar upward until it separates from the casing of the front panel. Pull the display board out of the front panel.
4. Remove Switch Pad — The conductive rubber switch pad simply pulls out of the front panel.

3.7 Cooling fan removal

The cooling fan, which is mounted to the rear panel of the chassis (see drawing 2001-060), does not need to be removed in order to clean the filter. To clean the filter, refer to paragraph 1.4. If, however, the fan needs to be removed, perform the following procedure.

NOTE

In order to remove the cooling fan, the case cover must be removed (see paragraph 3.4.1) and the analog board must be removed (see paragraph 3.5.3).

1. Disconnect Fan Cable — Turn the chassis upside-down and unplug the fan cable from connector J1037. This two conductor cable connection is located at the rear of the digital board in front of the IEEE connector. Return the chassis to the right-side-up position.
2. Remove Mounting Nuts— The fan is secured to the chassis by two mounting nuts. Remove these nuts and pull the fan out of the chassis.

3.8 Main CPU firmware replacement

Changing the firmware may be necessary as upgrades become available. The firmware revision level for the main CPU is displayed during the power-on sequence. The firmware for the main CPU is located in EPROM

U611, a leadless IC which resides in a chip carrier on the digital board.

Perform the following steps to replace the CPU firmware:

WARNING

Disconnect the instrument from the power line and remove all test leads before changing the firmware.

1. Remove the case cover as explained in paragraph 3.4.1.
2. Turn the instrument upside down to gain access to the digital board.
3. Locate U611 (EPROM) on the digital board. It is the only device installed in a chip carrier (socket).

CAUTION

EPROM U611 is a static sensitive device. Be sure to adhere to the handling precautions explained in paragraph 3.3.

4. Using an appropriate chip extractor, remove U611 from the chip carrier.
5. Position the new EPROM on the chip carrier. Make sure the notched corner of the chip is aligned with the notch in the chip carrier.
6. With the EPROM properly positioned, push down on the chip until it completely seats into the chip carrier.

3.9 Instrument re-assembly

The instrument can be re-assembled by reversing the previous disassembly procedures. Make sure that all parts are properly seated and secured, and that all connections are properly made. To ensure proper operation, shields must be replaced and fastened securely.

WARNING

To ensure continued protection against safety hazards, verify that power line ground (green wire attached to AC power receptacle) and the power transformer ground are connected to the chassis.

3.10 Assembly drawings

The following assembly drawings are provided to assist in disassembly and re-assembly of the instrument. Also, the Keithley part numbers for most mechanical parts are provided in these drawings.

Front Panel Assembly; 2001-040

Analog Shield Assembly; 2001-050

Chassis Assembly (Analog Board); 2001-051

Chassis Assembly (Front Panel and Miscellaneous); 2001-052

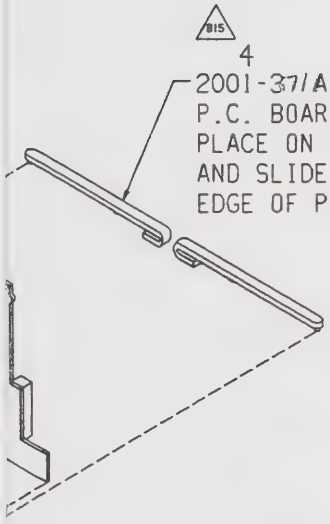
Chassis Assembly (Digital Board); 2001-053

Chassis Assembly (Case Cover and Handle); 2001-054

Chassis Assembly (Fan, Banana Jacks and Miscellaneous); 2001-060

REVISION	ENG	DATE
WAS 2001-318E	ST	5/10/94
WAS 2001-317F	ST	9/29/94
WAS 2001-110H	ST	11/9/94
WAS 2001-110H1	ST	1/24/95
WAS 2001-335D		

NO. 2001-040



PART NO.	QTY	
2001-370B	1	STAKI
2001-110H2	1	DISPL
2001-310A	1	OVERL
2001-317G	1	DISPL
2001-318F	1	CONDU
2001-371A	2	P.C.

2001	2001-052		1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY

USED ON

SCALE X

NG L.S.
PPR

TITLE
FRONT PANEL ASS'Y OP8

X

X

B

NO.
2001-040

ORIGINAL IF RED

U611, a leadless IC which resides in a chip carrier on the digital board.

Perform the following steps to replace the CPU firmware:

WARNING

Disconnect the instrument from the power line and remove all test leads before changing the firmware.

1. Remove the case cover as explained in paragraph 3.4.1.
2. Turn the instrument upside down to gain access to the digital board.
3. Locate U611 (EPROM) on the digital board. It is the only device installed in a chip carrier (socket).

CAUTION

EPROM U611 is a static sensitive device. Be sure to adhere to the handling precautions explained in paragraph 3.3.

4. Using an appropriate chip extractor, remove U611 from the chip carrier.
5. Position the new EPROM on the chip carrier. Make sure the notched corner of the chip is aligned with the notch in the chip carrier.
6. With the EPROM properly positioned, push down on the chip until it completely seats into the chip carrier.

3.9 Instrument re-assembly

The instrument can be re-assembled by reversing the previous disassembly procedures. Make sure that all parts are properly seated and secured, and that all connections are properly made. To ensure proper operation, shields must be replaced and fastened securely.

WARNING

To ensure continued protection against safety hazards, verify that power line ground (green wire attached to AC power receptacle) and the power transformer ground are connected to the chassis.

3.10 Assembly drawings

The following assembly drawings are provided to assist in disassembly and re-assembly of the instrument. Also, the Keithley part numbers for most mechanical parts are provided in these drawings.

Front Panel Assembly; 2001-040

Analog Shield Assembly; 2001-050

Chassis Assembly (Analog Board); 2001-051

Chassis Assembly (Front Panel and Miscellaneous); 2001-052

Chassis Assembly (Digital Board); 2001-053

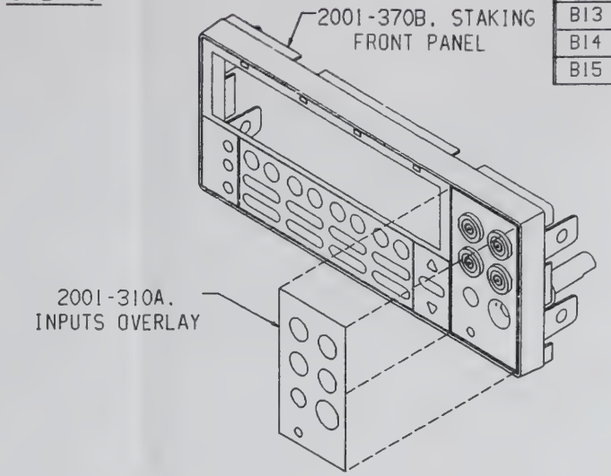
Chassis Assembly (Case Cover and Handle); 2001-054

Chassis Assembly (Fan, Banana Jacks and Miscellaneous); 2001-060

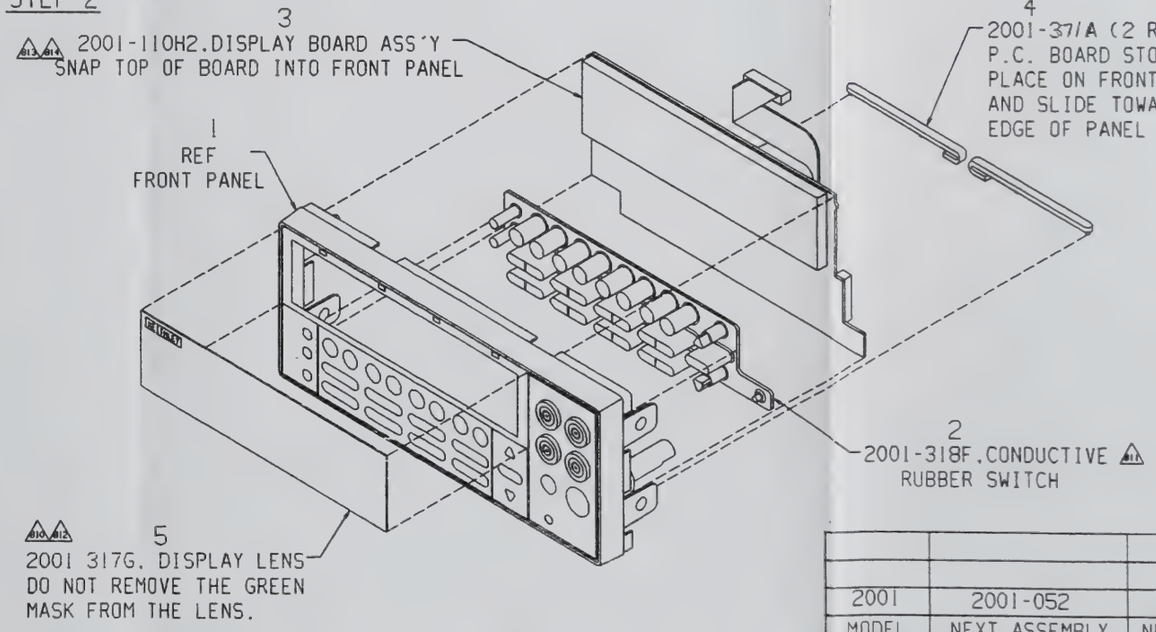
NO. 2001-040

LTR	ECA NO.	REVISION	ENG	DATE
B11	16454	2001-318F WAS 2001-318E	ST	5/10/94
B12	16610	2001-317G WAS 2001-317F	ST	9/29/94
B13	16802	2001-110H1 WAS 2001-110H	ST	11/9/94
B14	16924	2001-110H2 WAS 2001-110H1	ST	1/24/95
B15	17073	2001-370B WAS 2001-335D		

STEP 1



STEP 2



PART NO.	QTY	DESCRIPTION	
2001-370B	1	STAKING. FRONT PANEL	
2001-110H2	1	DISPLAY BOARD ASS'Y	△13,△14
2001-310A	1	OVERLAY	
2001-317G	1	DISPLAY LENS	△12
2001-318F	1	CONDUCTIVE RUBBER SWITCH	△11
2001-371A	2	P.C. BD STOP	△15

2001	2001-052		1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY

USED ON

DO NOT SCALE THIS DRAWING

KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139

DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED

XX ± .015 ANG ± 1°

XXX ± .005 FRAC ± 1/64

SURFACE MAX 63

DATE 1/13/94 | DRN Mat | ENG APPR L.S.

SCALE X | MATERIAL X | FINISH X

TITLE FRONT PANEL ASS'Y 0P8

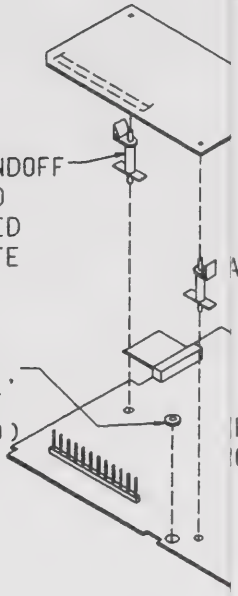
B | NO. 2001-040

ORIGINAL IF RED

050-1002	ON

REVISION	ENG	DATE
WAS 2001-100L1.	ST	6/17/94

STEP 1



ANALOG

F- ANALOG BOARD
OM STEP 1

REQUIRED PROCESS:
ST-202-1. STANDOFF. MUST RE
UNTIL INSERTION INTO ANALO
(PARTS CAN DRY & TURN BRIT
PRESS A/D BOARD INTO ST-202
PRESSURE APPLIED AT CORNER
TAB MUST NOT BE BENT BACK
TO CLEAR P.C. BOARD.

NSULATOR
OM SHIELD
SHIELD FIRST)

.ANALOG
HIELD

PART NO.	QTY	
2001-100M	1	ANALOG
2001-160J	1	A/D CO
2001-338C	1	ANALOG
2001-339C	1	ANALOG
2001-340B	1	INSULAT
GR-48-1	2	GROMME
MC-233A	2	LABEL,
ST-202-1	3	STANDO
#6-32x1-1/4"PPH	1	PHIL P
WA-54	1	FLAT W

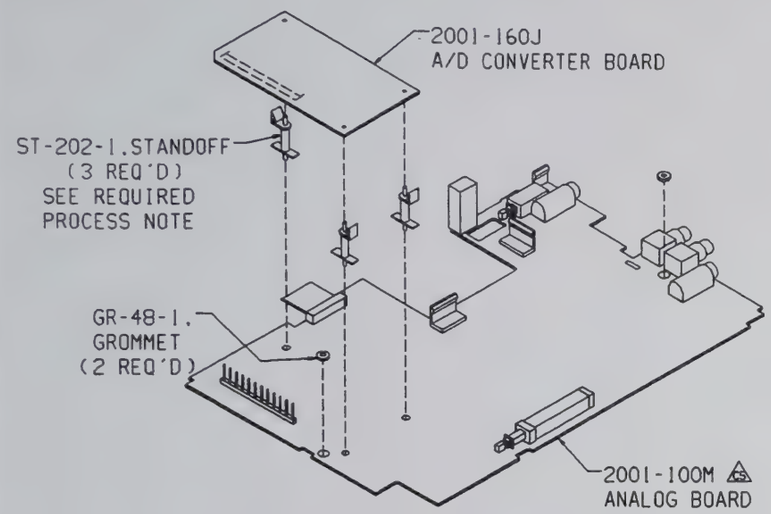
2001	2001-051B	CHASSIS ASS'Y	1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

ALE NONE	TITLE	
PR LS	ANALOG SHIELD ASS'Y - OP8	
	B	NO. 2001-050

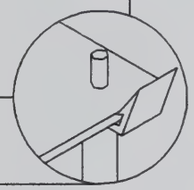
NO. 2001-050

LTR	ECA NO.	REVISION	ENG	DATE
C5	16440	2001-100M WAS 2001-100L1.	ST	6/17/94

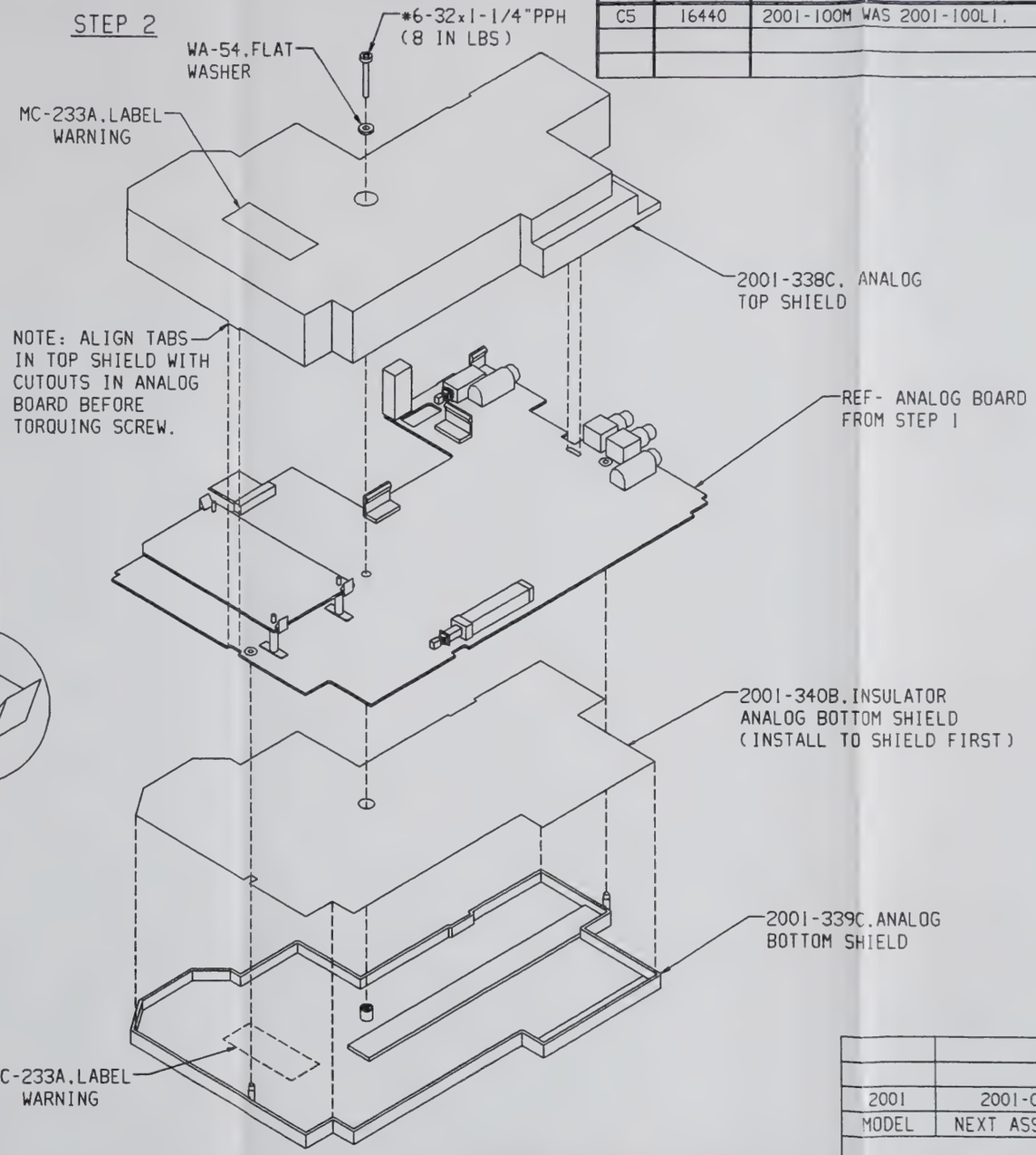
STEP 1



REQUIRED PROCESS:
ST-202-1, STANDOFF, MUST REMAIN IN SEALED PLASTIC BAG UNTIL INSERTION INTO ANALOG BOARD ASSEMBLY. (PARTS CAN DRY & TURN BRITTLE.)
PRESS A/D BOARD INTO ST-202-1's ONE AT A TIME WITH PRESSURE APPLIED AT CORNER OF P.C. BOARD ONLY. TAB MUST NOT BE BENT BACK MORE THAN IS NECESSARY TO CLEAR P.C. BOARD.



STEP 2



PART NO.	QTY	DESCRIPTION
2001-100M	1	ANALOG BOARD
2001-160J	1	A/D CONVERTER BOARD
2001-338C	1	ANALOG TOP SHIELD
2001-339C	1	ANALOG BOTTOM SHIELD
2001-340B	1	INSULATOR, ANALOG BOTTOM SHIELD
GR-48-1	2	GROMMET
MC-233A	2	LABEL, WARNING
ST-202-1	3	STANDOFF, EDGE HOLDING
#6-32x1-1/4"PPH	1	PHIL PAN HD SCREW
WA-54	1	FLAT WASHER

2001	2001-051B	CHASSIS ASS'Y	1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

DO NOT SCALE THIS DRAWING

KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139

DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED
XX = ±.015 ANG = ±1°
XXX = ±.005 FRAC = ±1/64
SURFACE MAX 63

DATE 3/18/92 SCALE NONE
DRN KAS ENG APPR LS
MATERIAL
FINISH

TITLE ANALOG SHIELD ASS'Y - OP8

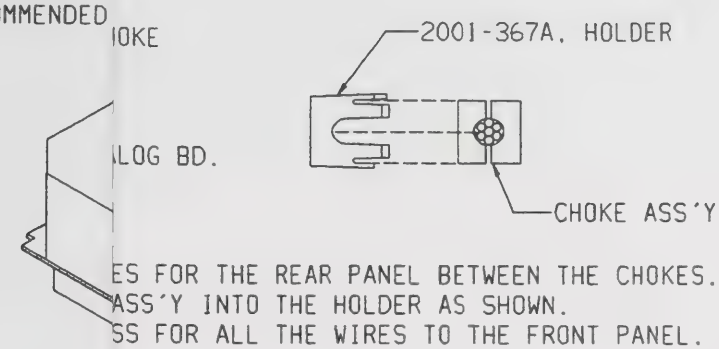
B NO. 2001-050

NO. 2001-051	REVISION	ENG	DATE
	WAS 2001-353B	ST	5/10/94
	WAS 2001-343B	ST	6/17/94

STEP 1

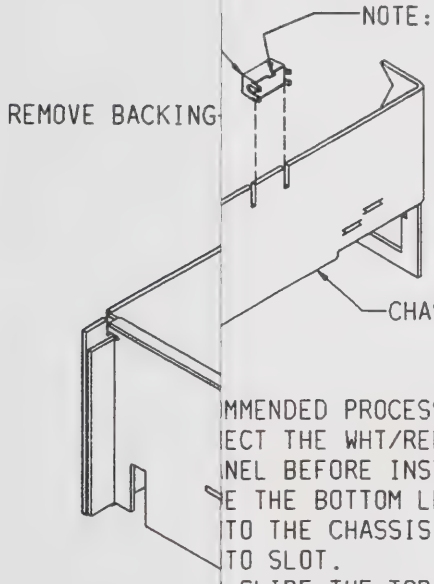
2001-05
ANALOG/ADC
SEE RECOMMENDED

IOKE



ES FOR THE REAR PANEL BETWEEN THE CHOKES.
ASS'Y INTO THE HOLDER AS SHOWN.
SS FOR ALL THE WIRES TO THE FRONT PANEL.

"A" BEFORE INSTALLING



MMENDED PROCESS:
ECT THE WHT/RED AND WHT/YEL WIRES TO REAR
NEL BEFORE INSTALLING THE CHOKE HOLDER.
E THE BOTTOM LEG ON ONE SIDE OF HOLDER
TO THE CHASSIS. THEN SLIDE THE OTHER LEG
TO SLOT.
SLIDE THE TOP LEGS INTO THE CHASSIS SLOTS
SLIGHTLY PRESSING INWARD.

2001-061
CHASSIS/BJ ASS'Y

PART NO.	QTY	
2001-061	1	CHASS
2001-353C	1	FILTE
2001-343C	1	CLIP.
2001-050	1	ANALO
CH-58-1A	4	CHOKE
2001-367A	2	HOLDE
1/2THINLKWA	2	THIN
FA-234-1	2	1/2-2

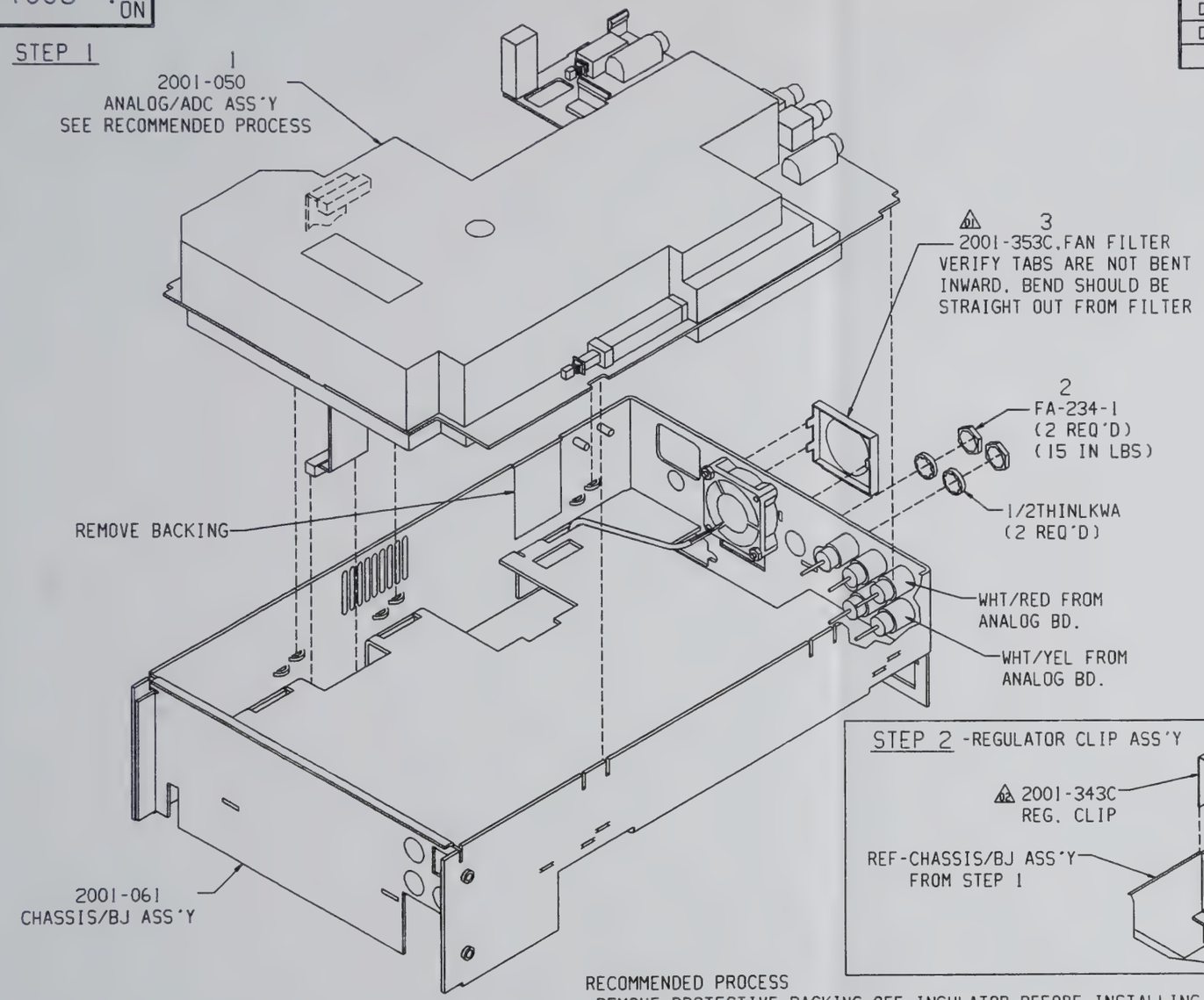
2001	2001-052B	CHASSIS ASSEMBLY	1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

SCALE NONE	TITLE	CHASSIS ASSEMBLY - OP8 (ANALOG SIDE)
APPR LS		
	B	NO. 2001-051

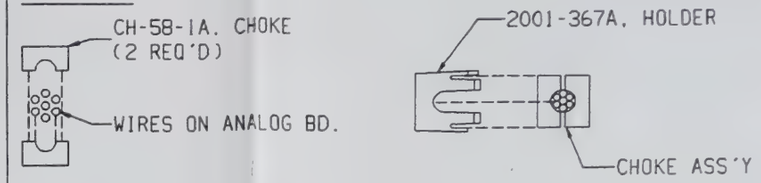
NO. 2001-051

LTR	ECA NO.	REVISION	ENG	DATE
D1	16454	2001-353C WAS 2001-353B	ST	5/10/94
D2	16440	2001-343C WAS 2001-343B	ST	6/17/94

STEP 1

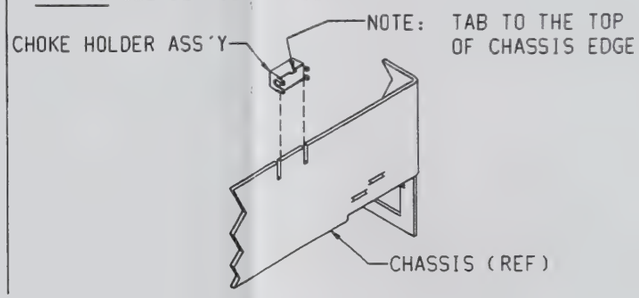


DETAIL "A"



PLACE ALL THE WIRES FOR THE REAR PANEL BETWEEN THE CHOKES.
SLIDE WIRE/CHOKE ASS'Y INTO THE HOLDER AS SHOWN.
DO THE SAME PROCESS FOR ALL THE WIRES TO THE FRONT PANEL.

STEP 3 SEE DETAIL "A" BEFORE INSTALLING



STEP 2 -REGULATOR CLIP ASS'Y

RECOMMENDED PROCESS:
CONNECT THE WHT/RED AND WHT/YEL WIRES TO REAR PANEL BEFORE INSTALLING THE CHOKE HOLDER.
SLIDE THE BOTTOM LEG ON ONE SIDE OF HOLDER INTO THE CHASSIS. THEN SLIDE THE OTHER LEG INTO SLOT.
THEN SLIDE THE TOP LEGS INTO THE CHASSIS SLOTS BY SLIGHTLY PRESSING INWARD.

RECOMMENDED PROCESS
REMOVE PROTECTIVE BACKING OFF INSULATOR BEFORE INSTALLING BOARD ASS'Y.
PLACE CONNECTORS ON ANALOG BOARD SLIGHTLY INTO HOLES IN CHASSIS.
PLACE RIBBON CABLE THRU CUTOUT IN CHASSIS.
ALIGN BOARD SLOTS WITH LANCES ON CHASSIS.
SLIDE BOARD TOWARD REAR PANEL, BEING CAREFUL NOT TO PINCH WIRES FROM FAN.

PART NO.	QTY	DESCRIPTION
2001-061	1	CHASSIS/BJ ASS'Y
2001-353C	1	FILTER, FAN
2001-343C	1	CLIP, REGULATOR
2001-050	1	ANALOG/ADC ASS'Y
CH-58-1A	4	CHOKE
2001-367A	2	HOLDER
1/2THINLKWA	2	THIN LOCKWASHER
FA-234-1	2	1/2-28 SMALL NUT

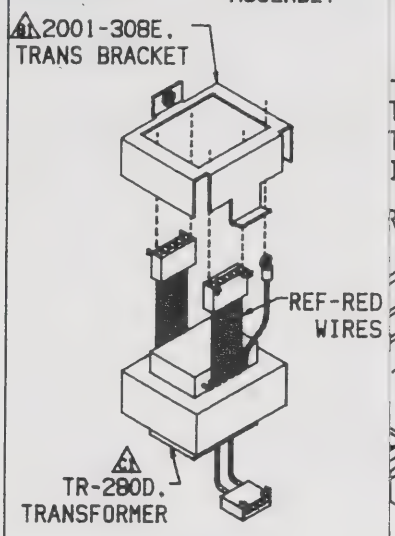
2001	2001-052B	CHASSIS ASSEMBLY	1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 9/16/93	SCALE NONE	TITLE CHASSIS ASSEMBLY - OP8 (ANALOG SIDE)
KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139	XX ± .015 ANG ± 1°	DRN KAS	ENG APPR LS	
	XXX ± .005 FRAC ± 1/64	MATERIAL	B	NO. 2001-051
	SURFACE MAX 63	FINISH		

2001-052 ON

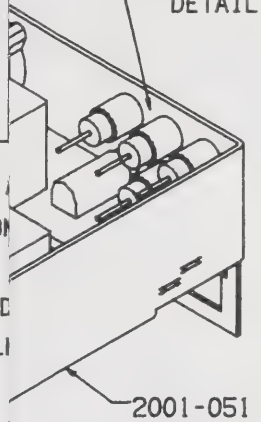
O.	REVISION	ENG.	DATE
	TR-280D WAS TR-280C. UNTWIST TRANSFORMER WIRES. LS	ZA	7-8-92
0	2001-312D WAS 2001-312C	SCM	7-9-92

DETAIL A - TRANSFORMER ASSEMBLY

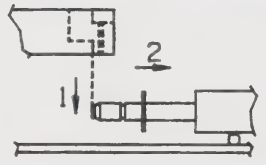


1
-004.
TER ASS'Y
TAIL C
IRING
RE
BLU WIRE

3
WIRE BJ's PER DETAIL B

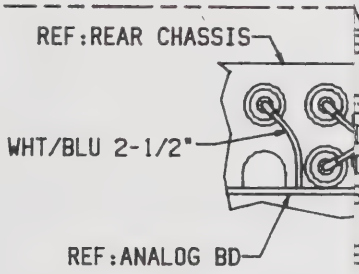


DETAIL D -SW ROD ASS'Y
SEE RECOMMENDED PROCESS



DETAIL B - BJ WIRING (FRONT PANEL
REF: FRON
RED
BLU
WHT

. FRONT/REAR SWITCH ROD
NDED PROCESS
SS SWITCH ON ANALOG BOARD.
SWITCH SHAFT THRU FRONT PANEL.
ETAIL D
IGN OPENING IN BOTTOM OF ROD OVER
ITCH SHAFT & EASE ROD DOWN.
SH ROD COMPLETELY ONTO SWITCH SHAFT.
SHOULD NOT BE WRAPPED AROUND PUSHROD.
ETAIL B FOR WIRE DRESS.



PART NO.	QTY
2001-051	1
2001-040	1
2001-004	1
2001-322A	1
2001-312D	1
2001-308E	1
TR-280D	1
FU-48	1
#6-32KEPNUT	2
#4-40x1/4"PPHSEM	1

CHASSIS ASS'Y
NEXT PROCESS STEP

2001	2001-053B	1
MODEL	NEXT ASSEMBLY	QTY.
USED ON		

ALE
G.
PR. LS

TITLE CHASSIS ASSEMBLY - OP8

SIZE B

NO. 2001-052

BRUNING 58425

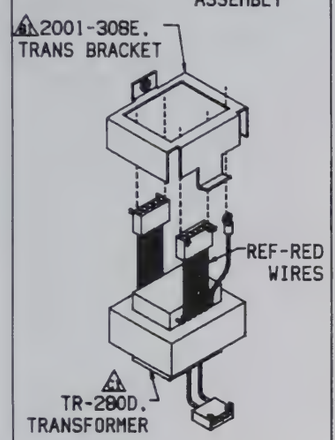
FORM 282778 REV. D

3-10

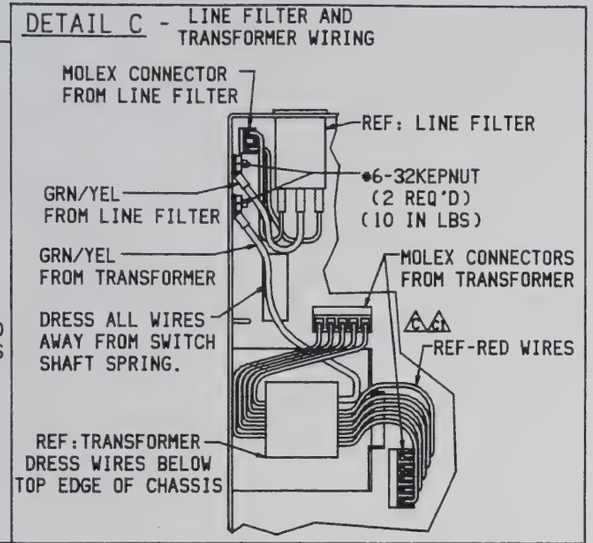
2001-052 ON

LTR.	ECO NO.	REVISION	ENG.	DATE
C1	15165	TR-280D WAS TR-280C. UNTWIST TRANSFORMER WIRES. ES	LK	7-5-92
C2	15290	2001-312D WAS 2001-312C	SCM	7-9-92

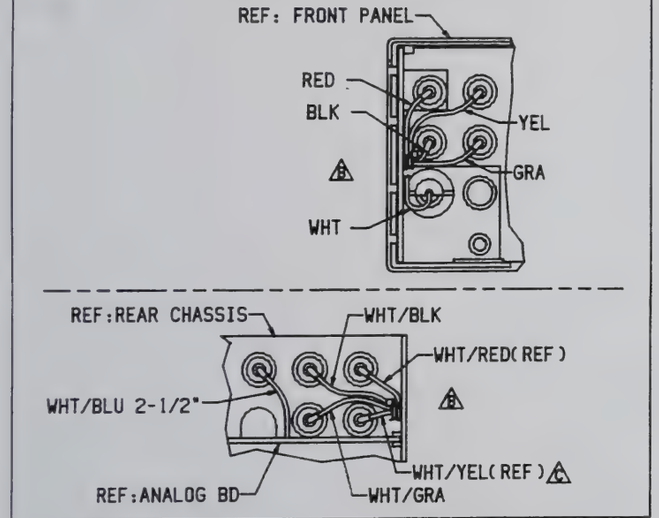
DETAIL A - TRANSFORMER ASSEMBLY



DETAIL C - LINE FILTER AND TRANSFORMER WIRING



DETAIL B - BJ WIRING (FRONT PANEL AND REAR CHASSIS)



6
TRANSFORMER ASS'Y FROM DETAIL A
SEE DETAIL C FOR WIRING
(NOTE: WHERE WIRES COME OUT OF THE TRANSFORMER, DRESS WIRES DOWN AND NEXT TO TRANSFORMER WINDING.)

1
2001-004.
LINE FILTER ASS'Y
SEE DETAIL C
FOR WIRING

BRN WIRE
BLU WIRE

#4-40x1/4"PPHSEM
(7 IN LBS)

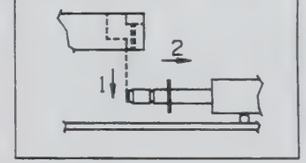
3
WIRE BJ's PER DETAIL B

2
2001-040
FRONT PANEL ASS'Y
SEE DETAIL B
FOR WIRING

2001-051
CHASSIS ASS'Y

4
2001-322A. FRONT/REAR SWITCH ROD
RECOMMENDED PROCESS
DEPRESS SWITCH ON ANALOG BOARD.
PLACE SWITCH SHAFT THRU FRONT PANEL.
SEE DETAIL D
1) ALIGN OPENING IN BOTTOM OF ROD OVER SWITCH SHAFT & EASE ROD DOWN.
2) PUSH ROD COMPLETELY ONTO SWITCH SHAFT.
WIRES SHOULD NOT BE WRAPPED AROUND PUSHROD.
SEE DETAIL B FOR WIRE DRESS.

DETAIL D -SW ROD ASS'Y
SEE RECOMMENDED PROCESS



FU-48. FUSE

3
WIRE BJ's PER DETAIL B.
ANY EXCESS OF WIRE SHOULD BE DRESSED TOWARD CENTER OF UNIT AND BELOW EDGE OF CHASSIS.

5
2001-312D, JACK.
CURRENT INPUT

PART NO.	QTY	DESCRIPTION
2001-051	1	CHASSIS ASS'Y
2001-040	1	FRONT PANEL ASS'Y
2001-004	1	WIRE CRIMP (LINE FILTER ASS'Y)
2001-322A	1	FRONT/REAR SWITCH ROD
2001-312D	1	JACK, CURRENT INPUT
2001-308E	1	TRANSFORMER BRACKET
TR-280D	1	TRANSFORMER
FU-48	1	FUSE, 2 AMP
#6-32KEPNUT	2	KEPNUT
#4-40x1/4"PPHSEM	1	PHIL PAN HD SEMS SCREW

CHASSIS ASS'Y
NEXT PROCESS STEP

MODEL	NEXT ASSEMBLY	QTY.
2001	2001-053B	1

USED ON

DO NOT SCALE THIS DRAWING

DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED
XX = ± .015 ANG. = ±1°
XXX = ± .005 FRAC. = ±1/64
SURFACE MAX. 63

DATE 11/20/91 SCALE ~
DRN. RAS ENG. APPR. LS
MATERIAL ~
FINISH ~

KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139

TITLE CHASSIS ASSEMBLY - OP8

SIZE B NO. 2001-052

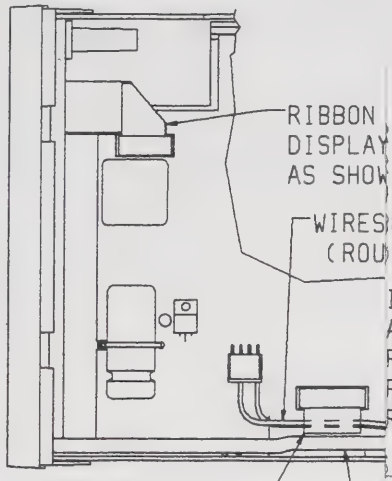
BRUNING 58425 FORM 282778 REV. D

3-10

2001-053 ON

REVISION	ENG	DATE
-140K4, 2001-803B07 WAS 2001-803B06. -804B06.	ST	3/14/94
01-803B07 AND 2001-804B08 WAS 2001-804B07.	ST	10/10/94
01-803B08 AND 2001-804B09 WAS 2001-804B08.	ST	7/7/95

DETAIL A - DIGITAL BOA



PUSHROD
B

U FRONT PANEL(PUSH DOWN SLIGHTLY
EDGE OF FRONT PANEL).
D THRU CUTOUT IN CHASSIS TO
OARD.
TO INSTALL ON SWITCH(SEE DETAIL).

ITAL BOARD ASS'Y △4△5△6
A FOR WIRING)
ROM (REF)
ROM (REF) △5△6
ROM (REF)

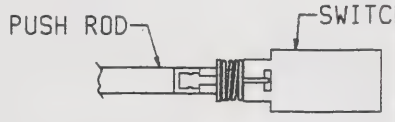
REDGE OF CHASSIS.
WITH LANCES ON CHASSIS, BEING
NCH FAN WIRE, TRANSFORMER WIRES.

S REAR PANEL, AGAIN CHECKING FAN WIRE.
D DOWN TO SNAP INTO PLACE ON LONG

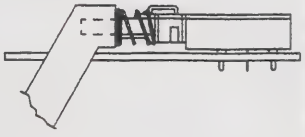
EQ'D. IN CONNECTORS ON REAR PANEL.
HASSIS BEFORE TIGHTENING THE CONNECTORS
..

DETAIL B PROPERLY INSTALLE
PUSH ROD

TOP VIEW



SIDE VIEW



CREWLOCK, FEMALE
(5 IN LBS)

E HARDWARE KIT
BS)

RECOMMENDED PROCESS FOR ANAL
PULL RIBBON CABLE STRAIGHT
PLUG CABLE INTO CONNECTOR T
PUSH EXCESS DOWN INTO CHASS
THE SIDE.
MAKE SURE PUSHROD IS NOT RU

PART NO.	QTY	
2001-052	1	CHA
2001-140K7	1	DIG
2001-320A	1	POW
CS-713	1	IEE
CS-725	2	SCR
#4-40x1/4"PPHSEM	5	PHI

01	2001-054	CHASSIS ASS'Y	1
DEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

E
LS

TITLE
CHASSIS ASSEMBLY - OP8

B

NO.
2001-053

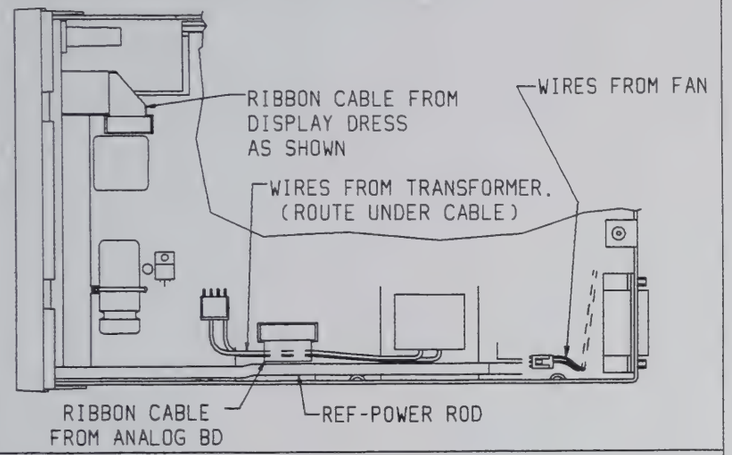
ORIGINAL IF RED

3-11

NO. 2001-053

LTR	ECA NO.	REVISION	ENG	DATE
C4	16409	2001-140K5 WAS 2001-140K4. 2001-803B07 WAS 2001-803B06. 2001-804B07 WAS 2001-804B06.	ST	3/14/94
C5	16766	2001-803B08 WAS 2001-803B07 AND 2001-804B08 WAS 2001-804B07.	ST	10/10/94
C6	17540	2001-803B09 WAS 2001-803B08 AND 2001-804B09 WAS 2001-804B08.	ST	7/7/95

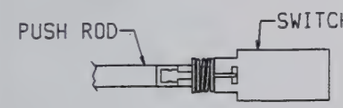
DETAIL A - DIGITAL BOARD WIRING



DETAIL B

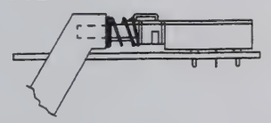
PROPERLY INSTALLED PUSH ROD

TOP VIEW



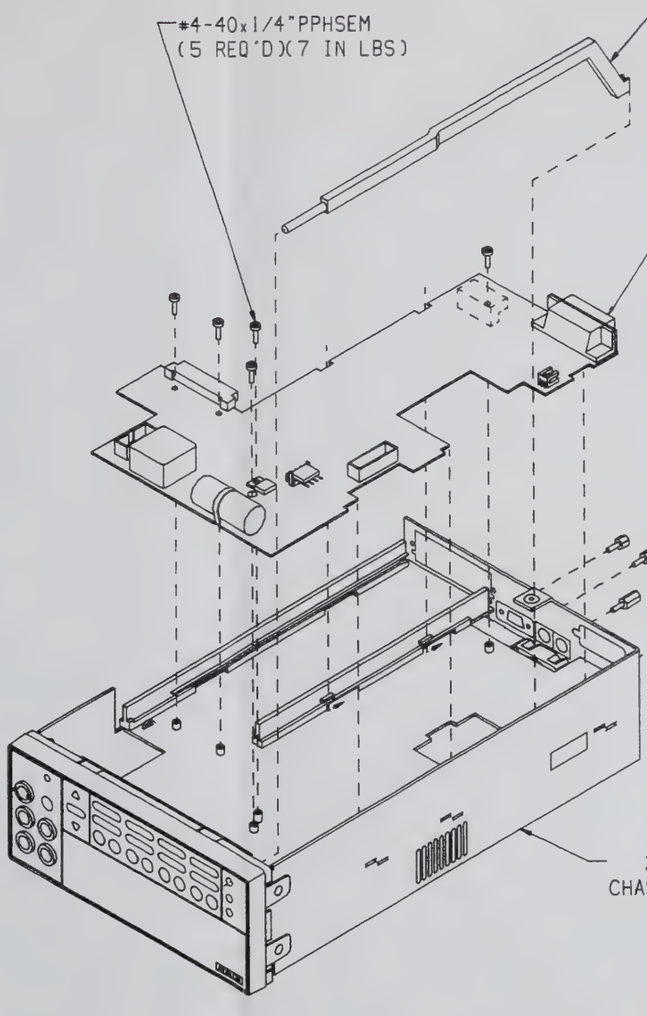
PUSH TOP OF SWITCH SHAFT DOWN INTO PUSHROD UNTIL IT BOTTOMS OUT.

SIDE VIEW



PRESS UPWARD ON PUSHROD WHILE PUSHING SWITCH SHAFT DOWN

RECOMMENDED PROCESS FOR ANALOG RIBBON CABLE
- PULL RIBBON CABLE STRAIGHT UP (EXCESS LENGTH ON THIS SIDE).
- PLUG CABLE INTO CONNECTOR THEN FOLD SLIGHTLY TOWARDS CONNECTOR.
- PUSH EXCESS DOWN INTO CHASSIS. BUT DO NOT BLOCK VENT HOLES ON THE SIDE.
- MAKE SURE PUSHROD IS NOT RUBBING ON CABLE.



RECOMMENDED PROCESS
- PLACE POWER ROD THRU FRONT PANEL(PUSH DOWN SLIGHTLY ON ROD TO GO UNDER EDGE OF FRONT PANEL).
- PUT OTHER END OF ROD THRU CUTOUT IN CHASSIS TO SWITCH ON ANALOG BOARD.
- PRESS UPWARD ON ROD TO INSTALL ON SWITCH(SEE DETAIL).

2001-140K7.DIGITAL BOARD ASS'Y △△CS△△ (SEE DETAIL A FOR WIRING)
2001-801A05 EPROM (REF)
2001-803B09 EPROM (REF) △△C6△△
2001-804B09 EPROM (REF)

RECOMMENDED PROCESS
- PLACE FAN WIRE TO EDGE OF CHASSIS.
- ALIGN BOARD SLOTS WITH LANCES ON CHASSIS, BEING CAREFUL NOT TO PINCH FAN WIRE, TRANSFORMER WIRES, OR RIBBON CABLE.
- SLIDE BOARD TOWARDS REAR PANEL, AGAIN CHECKING FAN WIRE.
- PRESS EDGE OF BOARD DOWN TO SNAP INTO PLACE ON LONG CARD GUIDE.
- INSERT T-7584, 2 REQ'D, IN CONNECTORS ON REAR PANEL.
- TIGHTEN BOARD TO CHASSIS BEFORE TIGHTENING THE CONNECTORS TO THE REAR PANEL.

PART NO.	QTY	DESCRIPTION
2001-052	1	CHASSIS ASS'Y
2001-140K7	1	DIGITAL BD ASS'Y (REF 2001-801A05) △△CS△△
		(REF 2001-803B09) △△CS△△
		(REF 2001-804B09) △△CS△△
2001-320A	1	POWER PUSHROD
CS-713	1	IEEE HARDWARE KIT
CS-725	2	SCREWLOCK, FEMALE
#4-40x1/4"PPHSEM	5	PHIL PAN HD SEMS SCREW

2001	2001-054	CHASSIS ASS'Y	1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 12/5/91	SCALE	TITLE CHASSIS ASSEMBLY - OP8	
KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139	XX = ±.015 ANG = ±1°	DRN KAS	ENG APPR LS		
	XXX = ±.005 FRAC = ±1/64	MATERIAL		B	NO. 2001-053
	SURFACE MAX 63	FINISH			

ORIGINAL IF RED

3-11

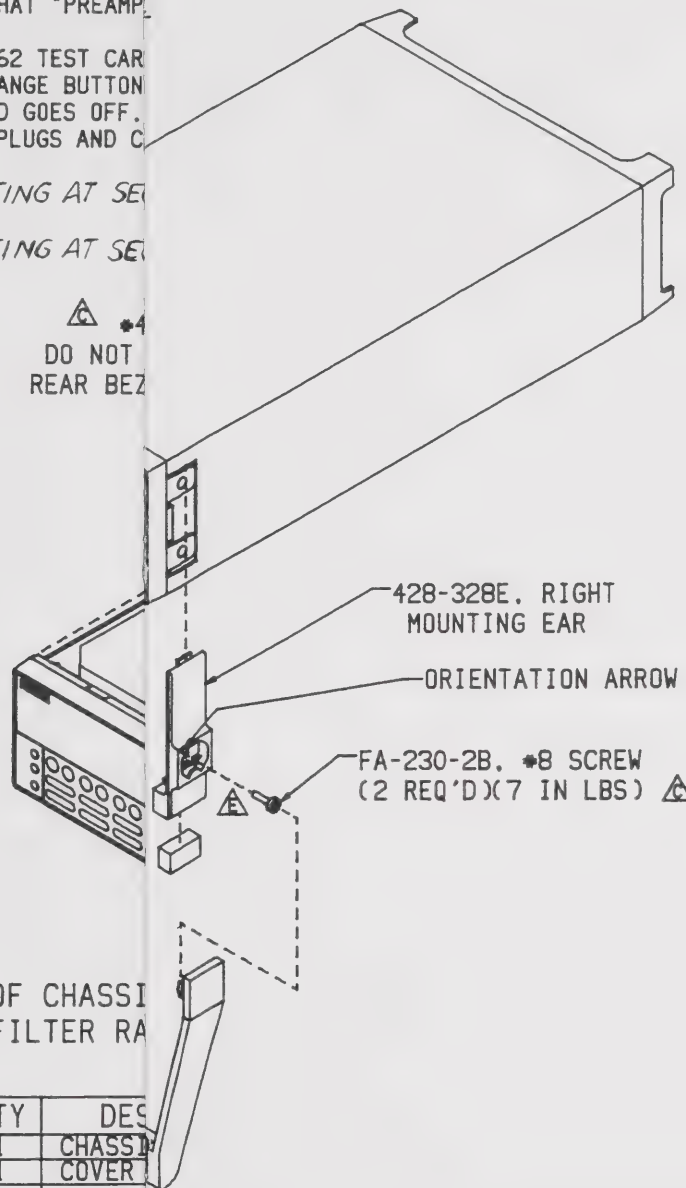
NO. 2001-054

REVISION	ENG	DATE
ASS'Y NOTES.	ST	5/4/93
3.3 WAS SEC 3.0 3.5 WAS SEC 3.0 AND SEC 3.5	ST	8/25/93

G BEFORE ASSEMBLY PERFORM

OPTION SLOT TEST
1) INSTALL 2001-762 OPTION SLOT
2) POWER ON. VERIFY THAT "PREAMP
ON LOWER DISPLAY.
3) VERIFY THAT 2001-762 TEST CAR
4) DEPRESS THE DOWN RANGE BUTTON
5) VERIFY THAT THE LED GOES OFF.
6) INSTALL TEMPORARY PLUGS AND C
DISPLAY BOARD TEST
1) SEE MS-1579. *STARTING AT SE*
BUILT IN TEST
1) SEE MS-1572. *STARTING AT SE*

G *4
DO NOT
REAR BEZ



ON REAR OF CHASSI
FOR FAN FILTER RA

PART NO.	QTY	DES
2001-053	1	CHASSI
2001-062	1	COVER
428-303D	1	REAR B
428-328E	1	MOUNTI
428-329F	1	HANDLE
428-338B	1	MOUNTI
FA-230-2B	2	FASTEN
FA-232-1C	2	CAPTIV
FE-22A	2	FOOT
#4-40x5/16"PFH	1	PHIL F

2001	2001-055B	FINAL CHASSIS ASS'Y	1
ODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

LE NONE	TITLE CHASSIS ASS'Y - OP8
LS	

	B	NO. 2001-054

NO. 2001-054

LTR	ECA NO.	REVISION	ENG	DATE
G	15828	REV BEFORE ASS'Y NOTES.	ST	5/4/93
G1	15960	STARTING AT SEC 3.3 WAS SEC 3.0 STARTING AT SEC 3.5 WAS SEC 3.0 AND SEC 3.5	ST	4/25/93

⚠6 BEFORE ASSEMBLY PERFORM

OPTION SLOT TEST ⚠1

1) INSTALL 2001-762 OPTION SLOT TEST CARD.
2) POWER ON. VERIFY THAT "PREAMP ON" APPEARS ON LOWER DISPLAY.
3) VERIFY THAT 2001-762 TEST CARD LED IS ON. ⚠2
4) DEPRESS THE DOWN RANGE BUTTON ONCE.
5) VERIFY THAT THE LED GOES OFF.
6) INSTALL TEMPORARY PLUGS AND COVER PLATE.

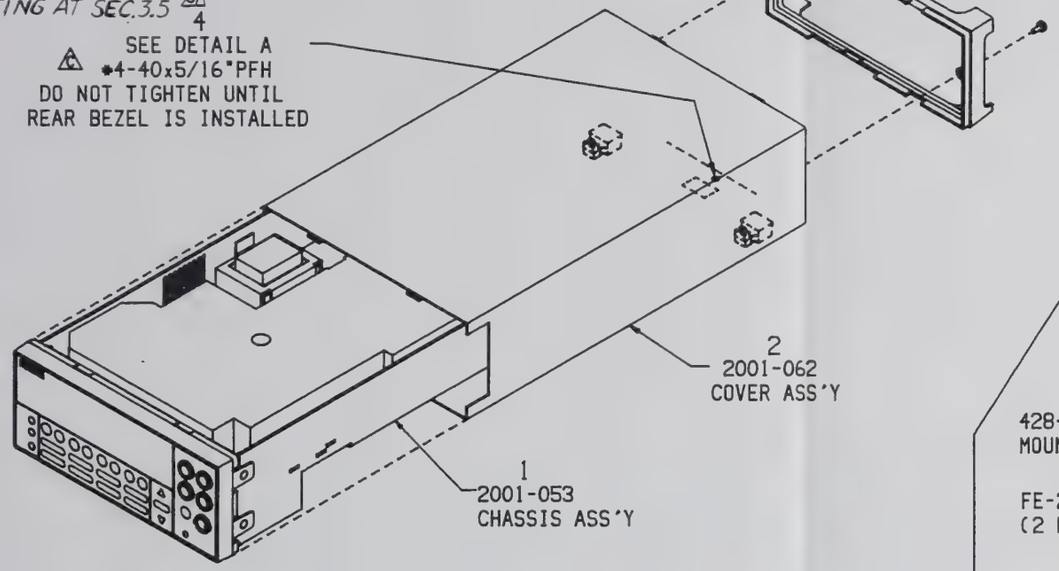
DISPLAY BOARD TEST

1) SEE MS-1579. *STARTING AT SEC. 3.3* ⚠G1

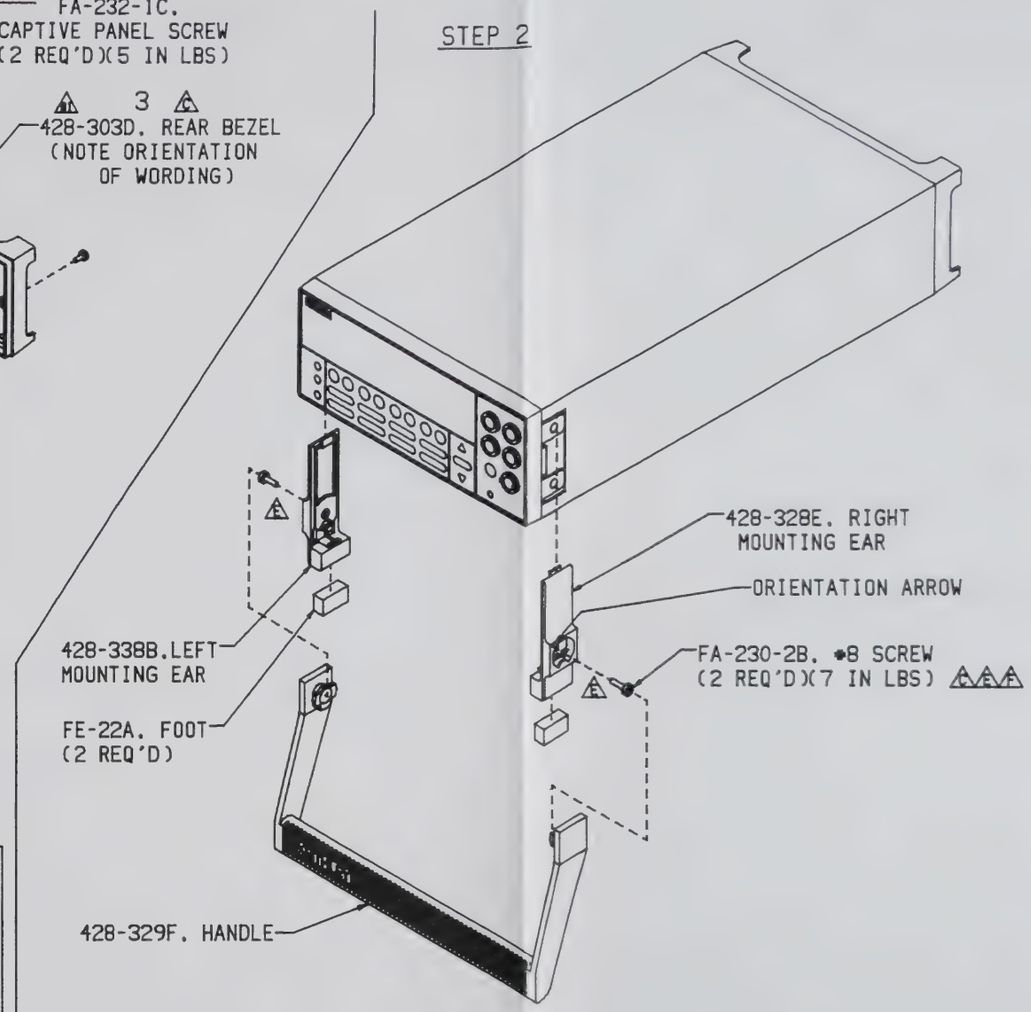
BUILT IN TEST

1) SEE MS-1572. *STARTING AT SEC. 3.5* ⚠G1

STEP 1



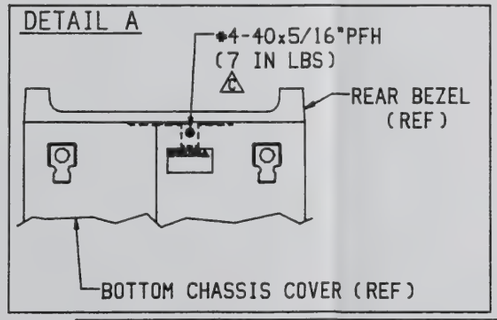
STEP 2



ON REAR OF CHASSIS CHECK FOR FAN FILTER RATTLE

PART NO.	QTY	DESCRIPTION	
2001-053	1	CHASSIS ASS'Y	
2001-062	1	COVER ASS'Y	
428-303D	1	REAR BEZEL	⚠1
428-328E	1	MOUNTING EAR RIGHT	
428-329F	1	HANDLE	
428-338B	1	MOUNTING EAR LEFT	
FA-230-2B	2	FASTENER	⚠5
FA-232-1C	2	CAPTIVE PANEL SCREW	
FE-22A	2	FOOT	
			⚠4⚠4
#4-40x5/16"PFH	1	PHIL FLAT HD SCREW	⚠5

DETAIL A



2001	2001-055B	FINAL CHASSIS ASS'Y	1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 12/5/91	SCALE NONE	TITLE CHASSIS ASS'Y - OP8
KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139	XX = ±.015 ANG = ±1°	DRN KAS	ENG APPR LS	
	XXX = ±.005 FRAC = ±1/64	MATERIAL	B	NO. 2001-054
	SURFACE MAX 63	FINISH		

NO. 2001-060

REVISION	ENG	DATE
AS 2001-305K	SF	3/22/84

s.
AFTER PRESSING.

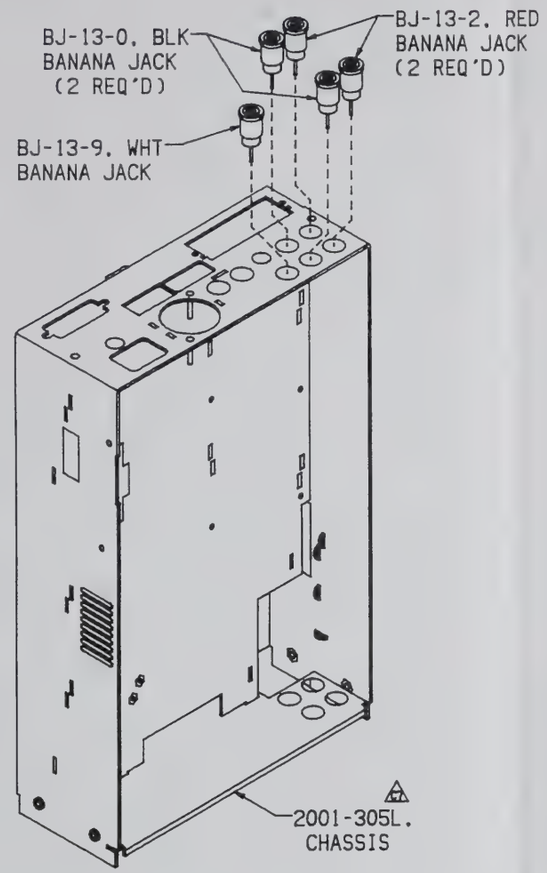
PART NO.	QTY	
2001-305L	1	CHAS
BJ-13-0	2	BANA
BJ-13-2	2	BANA
BJ-13-9	1	BANA

002	2001-061B	CHASSIS ASS'Y	1
001	2001-061B	CHASSIS ASS'Y	1
DEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

LE NONE	TITLE CHASSIS BJ ASSEMBLY
LS	
	B NO. 2001-060

NO. 2001-060

LTR	ECA NO.	REVISION	ENG	DATE
C7	16373	2001-305L WAS 2001-305K	SF	3/20/94



NOTES:
USE T-7539 WHEN PRESSING IN BJ's.
BJ's MUST BE STRAIGHT AND FLUSH AFTER PRESSING.
DO NOT BEND CHASSIS.

PART NO.	QTY	DESCRIPTION
2001-305L	1	CHASSIS
BJ-13-0	2	BANANA JACK, BLK
BJ-13-2	2	BANANA JACK, RED
BJ-13-9	1	BANANA JACK, WHT

2002	2001-061B	CHASSIS ASS'Y	1
2001	2001-061B	CHASSIS ASS'Y	1
MODEL	NEXT ASSEMBLY	NEXT PROCESS STEP	QTY
USED ON			

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 11/13/91	SCALE NONE	TITLE CHASSIS BJ ASSEMBLY
KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139	XX - ±.015 ANG - ±1°	DRN KAS	ENG APPR LS	
	XXX - ±.005 FRAC - ±1/64	MATERIAL NONE	B	NO. 2001-060
	SURFACE MAX 63	FINISH NONE		

4

Replaceable Parts

4.1 Introduction

This section contains replacement parts information and component layout drawings for the Model 2001.

4.2 Parts lists

The following parts lists for the Model 2001 are integrated with the component layouts:

Table 4-1 A/D converter board parts list
Table 4-2 Analog board parts list
Table 4-3 Digital board parts list
Table 4-4 Display board parts list
Table 4-5 Miscellaneous parts list

Note: For part numbers to the various mechanical parts and assemblies, use the Miscellaneous parts list (Table 4-5) and the assembly drawings provided at the end of Section 3.

4.3 Ordering information

To place an order, or to obtain information concerning replacement parts, contact your Keithley representative or the factory (see inside front cover for addresses). When ordering parts, be sure to include the following information:

- Instrument model number (Model 2001)
- Instrument serial number
- Part description
- Circuit description (if applicable)
- Keithley part number

4.4 Factory service

If the instrument is to be returned to Keithley Instruments for repair, perform the following:

1. Call the Repair Department at 1-800-552-1115 for a Return Material Authorization (RMA) number.
2. Complete the service form at the back of this manual and include it with the instrument.
3. Carefully pack the instrument in the original packing carton.
4. Write ATTENTION REPAIR DEPARTMENT and the RMA number on the shipping label.

4.5 Component layouts

The component layouts are provided in the following pages and are integrated with the parts lists.

Table 4-1
Model 2001 A/D board, parts list

Circuit Desig.	Description	Keithley Part No.
	CHOKE 21-030-J	CH-55
	DIODE, ZENER, 6.4V, IN5479	DZ-73-1
	SOCKET, 68-PIN QUAD	SO-128-68
C800-805,807,809,815, 819,820,830	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
C808,818	CAP,1UF,20%,50V, CERAMIC	C-237-1
C812,814,824,826-829	CAP, 10UF,20%, 25V, TANTALUM (D7243)	C-440-10
C817	CAP, 150PF, 5%, 100V,CERAMIC (0805)	C-465-150P
C821	CAP,.33UF,10%, 50V CERAMIC (1812)	C-464-.33
C822,823	CAP, 27PF, 10%, 100V, CERAMIC(1206)	C-451-27P
C825	CAP, .01UF, 10%,100V POLYPROPYLENE	C-306-.01
C831	CAP, 33PF, 10%, 100V, CERAMIC (1206)	C-451-33P
CR801	DIODE, DUAL SWITCHING, BAV99L(SOT-23)	RF-82
P1026	CONNECTOR, FEMALE 25 PIN	CS-767-25
Q800	TRANS, PNP, MMBT3906L(SOT-23)	TG-244
Q801	TRANS, NPN, MMBT3904 (SOT-23)	TG-238
Q802-806,814	TRANS,N CHAN MOSPOW FET,2N7000 (TO-92)	TG-195
Q807,809,811	TRANS, SELECTED TG-128 (T0-92)	31841A
Q808,813	TRANS,N CHANNEL JFET,SELECTED J210	TG-167-1
Q810	TRANS,N CHANNEL JFET,5432 (TO-92)	TG-198
Q812	IC, +5V REGULATOR, 78L05AC, (T0-92)	IC-603
R800,813,838,839	RES, 100K, 5%, 125mW, METAL FILM (1206)	R-375-100K
R801	RES, 475, 1%, 125mW, METAL FILM (1206)	R-391-475
R802-805	RES, 2.21K, 1%, 125mW, METAL FILM (1206)	R-391-2.21K
R806,827	RES, 33.2K, 1%, 125mW, METAL FILM (1206)	R-391-33.2K
R808,811,812,859,862	RES,10K,5%,125MW,METAL FILM(1206)	R-375-10K
R810,820	RES, 2.7K, 5%, 125mW, METAL FILM (1206)	R-375-2.7K
R814	RES, 5.1K,5%, 125MW, METAL FILM (1206)	R-375-5.1K
R815,829	RES, 82.5, 1%, 125mW, METAL FILM (1206)	R-391-82.5
R818,823	RES, 2.74K, 1%, 1/8W,METAL FILM	R-88-2.74K
R819	RES, 18.7, 1%, 125mW, METAL FILM (1206)	R-391-18.7
R821,822,864	RES,1K,5%,125MW,METAL FILM(1206)	R-375-1K
R824,830	RES, 4.75K, 1%, 125mW, METAL FILM (1206)	R-391-4.75K
R826	RES,3.92K, 1%, 125mW, METAL FILM (1206)	R-391-3.92K
R828,861	RES, 26.7K, 1%, 125mW,METAL FILM (1206)	R-391-26.7K
R833-836	RES,1K,.1%,1/10W,METAL FILM	R-263-1K
R837,846	RES, 19K, .1%, 1/10W, METAL FILM	R-263-19K
R840	RES, 40K, .1%, 1/10W, METAL FILM	R-263-40K
R841	RES, 57.8K, .1%, 1/10W METAL FILM	R-263-57.8K
R842	RES, 920K, .1%, 1/10W METAL FILM	R-168-920K
R843	RES, 1.2K, .1%, 1/10W, METAL FILM	R-263-1.2K
R844	RES, 4.M, .1% 1/8W METAL FILM	R-402-4M

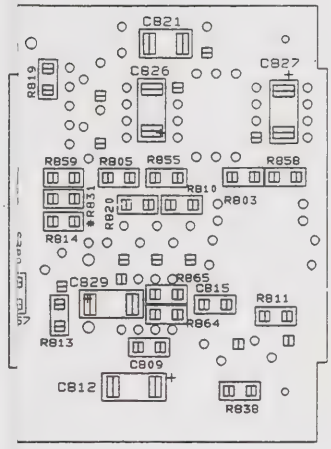
Table 4-1 (continued)
Model 2001 A/D board, parts list

Circuit Desig.	Description	Keithley Part No.
R845	RES,2K,.1%,1/10W,METAL FILM	R-263-2K
R847	RES, 3.2K,.1%, 1/10W, METAL FILM	R-263-3.2K
R848,851-853	RES, 49.9, 1%, 125mW, METAL FILM (1206)	R-391-49.9
R849,855,858,865	RES, 100, 1%, 125mW, METAL FILM (1206)	R-391-100
R850	RES,100,1%,1/8W,METAL FILM	R-88-100
R854	RES,1.62K,1%,1/8W,METAL FILM	R-88-1.62K
R856,857	RES,10,5%,125MW,METAL FILM(1206)	R-375-10
R860	RES, 150K, 5%, 125MW, METAL FILM (1206)	R-375-150K
R863	RES, 3.01K, 1%, 125MW, METAL FILM(1206)	R-391-3.01K
U800,801	IC, 8 STAGE SHIFT/STORE,MC14094BD(SOIC)	IC-772
U802	IC, OP-AMP, NE5534D (SOIC)	IC-802
U803,804	IC, VOLT. COMPARATOR,LM311M (SOIC)	IC-776
U806	IC, VOLT COMPARATOR LM393D(SOIC)	IC-775
U807	IC, QUAD COMPARATOR,LM339D (SOIC)	IC-774
U808	PROGRAM	2001-802-**
U809	IC,OP-AMP,OPA602AP	IC-703
U810,811	IC, OP-AMP,LT1097	IC-803
U812	IC, DUAL D-TYPE F/F, 74HC74(SOIC)	IC-773
U813	IC, OPA177GS (SOIC)	IC-960
VR801	DIODE,ZENER 6.4V,IN4579 (DO-7)	DZ-73
Y800	OSCILLATOR CMOS, 7.68 MHZ	CR-31

** Order present firmware revision level for main CPU (i.e., 2001-802-A05).

NO. 2001-160

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911015	RELEASED	MS	10/15/91
E1	14971	REVISED	S2	12/17/91
F	15061	ARTWORK REV WAS E. ADDED C831.	S2	1/17/92
G	15224	CHG'D ARTWORK FROM REV F TO G. ADDED R866-R863. ADDED 'DO NOT INSTALL' (SIDE -01).	AS	5/4/92
G1	15473	ADDED 2001-802805 UNDER U808.	S2	10/2/92
G2	15656	P1026 WAS P1036A.	AS	2/20/93
H	16152	ARTWORK WAS REV G. ADDED U811, R841 & R863. RELOCATED R811 TO SIDE -01 & R864 TO SIDE -04.		2/11/94
J	16466	CHG'D ARTWORK FROM REV H TO J.		



R831

-01)

N, REFER TO MODEL 2001 PRODUCT STRUCTURE.
STE STENCIL: 2001-168-04 REV J
: 2001-168.2-01 REV J

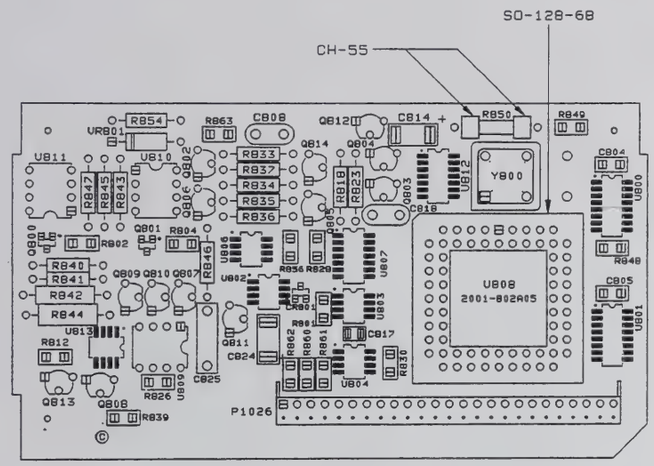
MODEL	NEXT ASSEMBLY	QTY.
USED ON		

RAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 10-12-91	SCALE 2:1	TITLE COMPONENT LAYOUT, A/D CONVERTER
MENTS INC. 44139	XX=±.015 ANG.=±1°	DRN. CB	ENG. APPR.	
	XXX=±.005 FRAC.=±1/64	MATERIAL	D	NO. 2001-160
	SURFACE MAX. 63	FINISH		

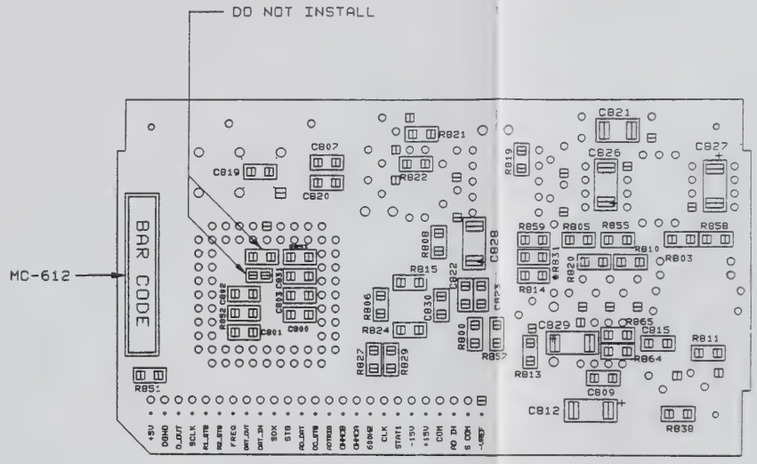
4-92

2001-160 DN

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911015	RELEASED	MS	10/15/91
E1	14971	REVISED	S2	12/17/91
F	15061	ARTWORK REV WAS E. ADDED C831.	S2	1/17/92
G	15224	CHG'D ARTWORK FROM REV F TO G. ADDED R866-[illegible] ADDED "DO NOT INSTALL" - SIDE -01.	AS	5/4/92
G1	15473	ADDED 2001-802A05 UNDER U808.	S2	10/2/92
G2	15656	P1026 WAS P1036A.	AS	2/20/93
H	16152	ARTWORK WAS REV G. ADDED VR[illegible] CHG'D [illegible] REVISED TO REV H. CHG'D TO SIDE -04.		2/11/94
J	16466	CHG'D ARTWORK FROM REV H TO J.		



COMPONENT SIDE (SIDE -04)



* DO NOT INSTALL R831

SOLDER SIDE (SIDE -01)

NOTES:
1. FOR COMPONENT INFORMATION, REFER TO MODEL 2001 PRODUCT STRUCTURE.
2. COMPONENT SIDE SOLDER PASTE STENCIL: 2001-168-04 REV J
3. SOLDER SIDE GLUE STENCIL: 2001-168.2-01 REV J

MODEL	NEXT ASSEMBLY	QTY.
	USED ON	

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 10-12-91	SCALE 2:1
KEITHLEY KEITHLEY INSTRUMENTS INC CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. CB	ENG. APPR.
	XXX=±.005 FRAC.=±1/64	MATERIAL	
	SURFACE MAX. 63	FINISH	

TITLE: COMPONENT LAYOUT, A/D CONVERTER

D | NO. 2001-160

4-80

Table 4-2
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
	COM CONN,TEST POINT	CS-553
	CONTACT, FUSE	2001-314
	FUSE HOLDER	FH-32
	HEAT SINK (USE WITH Q301,302,U102,107,108)	HS-41
	L.E.D. MOUNT (USE WITH Q529,530)	MK-21-1
	SPRING, COMPRESSION	SP-5
C100,111,113	CAP, 10UF,20%, 25V, TANTALUM (D7243)	C-440-10
C101,104	CAP, 2200UF, 20%, 35V ALUM ELEC	C-468-2200
C102	CAP, 2.2UF, 20%, 35V, TANTALUM (C6032)	C-476-2.2
C103	CAP,1UF, 20%, 50V, TANTALUM (1812)	C-431-1
C105, 118,119	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
C106	CAP, 2200UF, 20%, 16V ALUM ELEC	C-473-2200
C107	CAP,.01UF,20%,500V,CERAMIC	C-22-.01
C108	CAP, 1000UF, 20%, 50V ALUM ELEC	C-469-1000
C114,115	CAP, 470UF, 20%, 63V ALUM ELEC	C-477-470
C116,117	CAP, 1000UF, 20%,35V ALUM ELEC	C-468-1000
C201,202	CAP, .01uF, 20%, 50V, CERAMIC (1206)	C-418-.01
C203,204,200,205,218,220, 221	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
C206,207,208,211,212,219	CAP, 1000pF, 20%, 50V, CERAMIC (1206)	C-418-1000P
C209	CAP, 33PF, 10%, 100V, CERAMIC (1206)	C-451-33P
C210	CAP, 47PF, 10%, 100V, CERAMIC(1206)	C-451-47P
C213	CAP, 4.7PF, 5%, 50V, MONO-CERAMIC(0805)	C-452-4.7P
C214	CAP,100PF, 5%, 100V, CERAMIC(0805)	C-465-100P
C215	CAP, 150PF, 5%, 100V,CERAMIC (0805)	C-465-150P
C216	CAP, 6.2PF, .25PF, TOL, 1000V, CERAMIC	C-349-6.2P
C217	CAP, 1UF, 20%, 100V, CERAMIC	C-487-1
C306,307,347,348,350-353, 356-365	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
C316	CAP, 20PF, 5%, 500V, DIPPED MICA	C-236-20P
C320	CAP, 33PF, 10%, 100V, CERAMIC (1206)	C-451-33P
C322,324,326,327	CAP,.68uF, 20%,50V POLYESTER FILM	C-344-.68
C329	CAP,27PF,10%,200V,CERAMIC	C-451-27P
C330	CAP,.47UF,20%,50V,TANTALUM (1812)	C-431-.47
C336,337,341	CAP, 1000pF, 20%, 50V, CERAMIC (1206)	C-418-1000P
C343	CAP, 6800P, 5%, 100V, POLYESTER	C-424-6800P
C401,404,405,407,411-426, 428,430-433,435	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
C408	CAP,.15UF,20%,50V,CERAMIC(1206)	C-418-.15
C427	CAP, .01uF, 20%, 50V, CERAMIC (1206)	C-418-.01
C502,572	CAP, 10UF,20%, 25V, TANTALUM (D7243)	C-440-10
C504,570	CAP, 1000pF, 20%, 50V, CERAMIC (1206)	C-418-1000P
C513	CAP,2.2PF,.5%,1500V,CERAMIC	C-308-2.2P

Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
C522	CAP,10PF,10%,1000V,CERAMIC	C-64-10P
C529	CAP, 10000PF, 20%, 63V, POLY-FILM	C-471-10000P
C531	CAP,22PF,10%,1000V,CERAMIC	C-64-22P
C533,578	CAP,100PF,10%,1000V,CERAMIC	C-64-100P
C539,543,584-586,588-590, 597,599	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
C544,571,201,202,427	CAP, .01uF, 20%, 50V, CERAMIC (1206)	C-418-.01
C553	CAP, 820PF, 1%, 300V, GLASS	C-486-820P
C554	CAP, 91PF,1%,300V, MICA	C-474-91P
C555	CAP,3600PF, 1%, 500V,MICA	C-278-3600P
C556	CAP, 270PF, 1%, 300V, MICA	C-462-270P
C557	CAP, 10PF, 1%, 2000V GLASS	C-485-10P
C558	CAP, 6.2PF, .25PF, TOL, 1000V, CERAMIC	C-349-6.2P
C563	CAP, .1UF, 20%, 1000V, MET POLYCARB	C-490-.1
C566	CAP,1UF, 20%, 50V, TANTALUM (1812)	C-431-1
C569	CAP, 2.7pF, .25pF TOL, 1000V, CERAMIC	C-367-2.7P
C574	CAP, 27PF, 10%, 100V, CERAMIC(1206)	C-451-27P
C575,594	CAP,100PF,2.5%,630V,POLYPROPYLENE	C-405-100P
C576	CAP, 2.2UF,20%, 35V TANTALUM (C6032)	C-476-2.2
C579	CAP,47PF,10%,1000V,CERAMIC	C-64-47P
C580	CAP, 2.2UF, 20%, 63V, POLYCARB	C-480-2.2
C581-583	CAP, .33UF, 20%, 63V, POLYCARBONATE	C-482-.33
C587,591,595	CAP, 150PF, 5%, 100V,CERAMIC (0805)	C-465-150P
C593	CAP, 150PF, 5%, 100V,CERAMIC (0805)	C-465-150P
C598	CAP, 100UF, 20%, 10V, ALUM ELEC	C-483-100
CR100	DIODE, BRIDGE, 5 AMP/400V, EDI-PE40	RF-88
CR101,108	DIODE,BRIDGE,VM18	RF-52
CR102,103,113,114,117,118	DIODE, SWITCHING, 250MA,BAV103 (SOD-80)	RF-89
CR104	DIODE, DUAL SWITCHING, BAV99L(SOT-23)	RF-82
CR106	DIODE,SILICON,W04M (CASE WM)	RF-46
CR109-112	DIODE,CONTROLLED AVALANCHE,BYD17GSOD-87	RF-91
CR305	DIODE, BRIDGE PE05 (CASE KBU)	RF-48
CR309	DIODE, SILICON, 5400 (267-01)	RF-34
CR317,318	DIODE,SILICON,IN4006 (D0-41)	RF-38
CR321,323,324,327	DIODE, SWITCHING, MMBD914 (SOT-23)	RF-83
CR322	DIODE,CONTROLLED AVALANCHE,BYD17GSOD-87	RF-91
CR331-337	DIODE,IN3595 (DO-7)	RF-43
CR400-403	DIODE, SWITCHING, MMBD914 (SOT-23)	RF-83
CR501,504	DIODE, DUAL MIXER, MMBD352L (SOT-23)	RF-86
CR507,508,512,536,537	DIODE, SWITCHING, MMBD914 (SOT-23)	RF-83
CR509,510,518-520	DIODE,CONTROLLED AVALANCHE,BYD17GSOD-87	RF-91
CR511,523,524,535	DIODE, DUAL SWITCHING, BAV99L(SOT-23)	RF-82
CR513,514,521,526-528	DIODE, SWITCHING, 250MA,BAV103 (SOD-80)	RF-89
CR515,516	DIODE, SCHOTTKY, MMBD301 (SOT-23)	RF-90
CR517	DIODE,SILICON,IN4148 (DO-35)	RF-28
CR531-534,538,539	DIODE,IN3595 (DO-7)	RF-43
CR540,541	DIODE,SCHOTTKY, BAT42	RF-78

Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
E300	SURGE ARRESTOR, CG3-1.5L	SA-4
F100	FUSE, .5A, 250V	FU-71
F300	FUSE, 2A,250V, FAST-BLO(5X20MM)	FU-48
J1002	CONN, MOLEX, 3-PIN	CS-772-3
J1008-1011,J1017-1021	CRIMP CONTACT ROUND	CS-760
J1022,1023	CONN, BNC	CS-547
J1024,1025	CONN, MALE, 5-PIN (MOLEX 42491)	CS-784-5
J1026	HEADER, DUAL BODY/STRAIGHT PIN	CS-765-25
K100	RELAY, MINIATURE, G6A-274P-ST-US-DC24	RL-160
K101	RELAY, MINIATURE, G6A-274P-ST-US-DC9	RL-159
K300	RELAY,REED HI VOLTAGE	RL-119
K500,502,503	RELAY, REED, HI-VOLT/ISOLATION,848-1	RL-152
K501	RELAY, MINATURE (DPDT), DK1A1BE-6V	RL-153
L100	CHOKE, 100MHZ	CH-50
P1027	CABLE ASSEMBLY, 20 CONDUCTOR	CA-27-16C
Q101,106	TRANS, NPN, MMBT3904 (SOT-23)	TG-238
Q102,104	TRANS, N-MOSFET, VN0605T (SOT-23)	TG-243
Q103	TRANS, P-CHAN, MOSFET, TP0610T(SOT-23)	TG-259
Q105	TRANS, PNP, MMBT3906L(SOT-23)	TG-244
Q301	TRANS,NPN DARLINGTON, TIP101(TO 220)	TG-230
Q302	TRANS,PNP DARLINGTON, TIP106(TO 220)	TG-231
Q304,306,342	TRANS, N-CHAN JFET, SST109 (SOT-23)	TG-270
Q305,307	TRANS, N-HEXFET, IRFR020 (D-PAK)	TG-239
Q308,313	TRANS,N CHANNEL JFET (T0-92)	TG-225
Q309,310	TRANS, N-CHANNEL FET, BUZ71 (TO-220)	TG-196
Q311	TRANS,N CHANNEL JFET,5432 (TO-92)	TG-198
Q312,320,324,328,329	TRANS, SELECTED TG-128 (T0-92)	31841A
Q314,322,325	TRANS,NPN COMP SILICON AMP,2N5089	TG-62-1
Q315	TRANS, NPN, MMBT3904 (SOT-23)	TG-238
Q317	TRANS, N-CHAN JFET, SST4391 (SOT-23)	TG-250
Q321,323	TRANS,N-CHAN FET, BUK 456-1000B (TO-220)	TG-247
Q326	TRANS, PNP, MMBT3906L(SOT-23)	TG-244
Q330	TRANS, DUAL N-CHAN JFET, IFN146 (TO-71)	TG-254
Q331,333	SELECTED TG-166	2001-601A
Q337-340	TRANS,P-FET, MTP2N90	TG-232
Q341	TRANS, N-CHAN JFET, SST4393 (SOT-23)	TG-263
Q500,502-504,518-520,547, 550	TRANS, N-MOSFET, VN0605T (SOT-23)	TG-243
Q501,505,507-509,513, 516,522,523,538,544,551	TRANS, N-CHAN JFET, SST4416 (SOT-23)	TG-241

Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
Q506,511	TRANS,N-CHAN FET, BUK 456-1000B (TO-220)	TG-247
Q510	TRANS, N-CHAN JFET, SST4391 (SOT-23)	TG-250
Q512	TRANS, N-CHAN. DUAL JFET, U441	TG-235
Q514	TRANS, N-CHAN JFET SMP4338(SOT-23)	TG-257
Q515,517	TRANS, N-CHANNEL FET, J210(TO-92)	TG-176
Q525	TRANS,N CHANNEL JFET,SELECTED J210	TG-167-1
Q527	TRANS, SELECTED TG-128 (T0-92)	31841A
Q528	TRANS, N-CHAN MOSFET, MTG9N50E (TO-218)	TG-291
Q529,530	DIODE CURRENT REG CR200(T0-46)	TG-218
Q531,536,537	TRANS, PNP, MMBT3906L(SOT-23)	TG-244
Q532,540,545	TRANS, NPN, MMBT3904 (SOT-23)	TG-238
Q533	TRANS, N-CHAN DMOS FET TN2504N8 (SOT-89)	TG-261
Q534,535	TRANS, P-CHAN, MOSFET, TP0610T(SOT-23)	TG-259
Q539	TRANS, N-CHAN JFET, SST4393(SOT-23)	TG-263
Q542,546	TRANS, P CHANNEL JFET, J270 (TO-92)	TG-166-1
Q543	TRANS,CURRENT REGULATOR,CR430	TG-219
Q548,549	TRANS,N CHANNEL FET,2N4392 (TO-92)	TG-128-1
R100	RES, 470, 5%, 10W, VERTICAL MOUNT	R-401-470
R102,129	RES,243K, 1%, 125MW, METAL FILM(1206)	R-391-243K
R103	RES, 140K, 1%, 125MW, METAL FILM(1206)	R-391-140K
R104,117,120	RES, 499K, 1%, 125MW, METAL FILM(1206)	R-391-499K
R105	RES, 100K, 1%, 125mW, METAL FILM (1206)	R-391-100K
R107	RES, 562K, 1%, 125MW, METAL FILM (1206)	R-391-562K
R108	RES, 33, 5%, 250mW, METAL FILM (1210)	R-376-33
R109	RES, 475, 1%, 125mW, METAL FILM (1206)	R-391-475
R110	RES, 2.49K, 1%, 125MW, METAL FILM (1206)	R-391-2.49K
R111	RES, 59K, 1%,125MW,METAL FILM(1206)	R-391-59K
R114	RES, 1M, 5%, 1/2W, FLAME PROOF	R-394-1M
R116,118	RES, 20K, 5%, 125MW, METAL FILM (1206)	R-375-20K
R122	RES, 100K, 5%, 125mW, METAL FILM (1206)	R-375-100K
R123	RES, 20K, 5%, 250MW, METAL FILM (1210)	R-376-20K
R124-128	RES,10K,5%,125MW,METAL FILM(1206)	R-375-10K
R200	RES, 1.8M, 5%, 125MW, METAL FILM (1206)	R-375-1.8M
R201	RES, 1.2M, 5%, 125MW, METAL FILM(1206)	R-375-1.2M
R203,222	RES, 68K, 5%, 125MW METAL FILM (1206)	R-375-68K
R204,242,243,245,R267-269	RES, 200K, 5%, 125MW, METAL FILM(1206)	R-375-200K
R209,211,223,232,249,255	RES, 2K, 5%, 125MW, METAL FILM(1206)	R-375-2K
R210,277	RES, 137, 1%, 125MW, METAL FILM (1206)	R-391-137
R212,R235,238	RES, 20K, 5%, 125MW, METAL FILM (1206)	R-375-20K
R213	RES, 10K, 5%, 250MW, METAL FILM(1210)	R-376-10K
R214,225,251-253,256,280	RES,10K,5%,125MW,METAL FILM(1206)	R-375-10K
R215	RES NET, 500, 24.5K,0/1%, 125MW THIN FILM	TF-234
R216,217	RES, 15, 5%, 125MW, METAL FILM(1206)	R-375-15
R218,282	RES, 15K, 1%, 125mW, METAL FILM (1206)	R-391-15K
R219-221	RES, 120K, 5%, 125MW, METAL FILM(1206)	R-375-120K
R226,230	RES, 22K, 5%, 125MW, METAL FILM(1206)	R-375-22K

Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
R227,261-264,281,283,284, 288,289	RES,1K,5%,125MW,METAL FILM(1206)	R-375-1K
R228,240	RES,4.7K,5%,125MW,METAL FILM(1206)	R-375-4.7K
R229	RES, 470,5%, 125MW, METAL FILM(1206)	R-375-470
R231,286	RES, 620, 5%, 250mW, METAL FILM (1210)	R-376-620
R233,278	RES, 4.99K, 1%, 125mW,METAL FILM (1206)	R-391-4.99K
R234	RES, 220, 5%, 125MW, METAL FILM (1206)	R-375-220
R236	RES, 3.9M, 5%, 125MW, METAL FILM(1206)	R-375-3.9M
R237,254,265,266	RES, 1M, 5%, 125MW, METAL FILM (1206)	R-375-1M
R239,248,285	RES, 68, 5%, 125MW, METAL FILM(1206)	R-375-68
R241,248	RES, 1.5K, 5%, 250MW, METAL FILM(1210)	R-376-1.5K
R246,290	RES, 100K, 1%, 125mW, METAL FILM (1206)	R-391-100K
R247	RES, 680K, 5%,125mW, METAL FILM (1206)	R-375-680K
R257,258	RES, 100, 5%, 125MW, METAL FILM (1206)	R-375-100
R259,260,292	RES, 150, 5%, 125MW, METAL FILM (1206)	R-375-150
R270	RES, 2.7K, 5%, 125mW, METAL FILM (1206)	R-375-2.7K
R271-273	RES, 3.3K 5%, 125MW METAL FILM (1206)	R-375-3.3K
R274	RES,47K,5%,125MW,METAL FILM(1206)	R-375-47K
R275	RES,1K, 5% 250MW, METAL FILM (1210)	R-376-1K
R276,250	RES, 20K, 5%, 250MW, METAL FILM (1210)	R-376-20K
R279	RES, 665, 1%, 125MW, METAL FILM(1206)	R-391-665
R287	RES, 487K, 1%, 125mW, METAL FILM (1206)	R-391-487K
R291	RES, 3M, 5%, 125MW, METAL FILM (1206)	R-375-3M
R303-306,324	RES, 270,5%, 250mW, METAL FILM (1210)	R-376-270
R308,319	RES, 33, 5%, 250mW, METAL FILM (1210)	R-376-33
R309,318	RES,100K,1%,125mW,METAL FILM (1206)	R-391-100K
R316,317,333,337,361	RES,4.7K,5%,125MW,METAL FILM(1206)	R-375-4.7K
R326	RES, 9.09K, .1%, 1/10W, METAL FILM	R-263-9.09K
R327	RES, 46.4K, 1%, 1/8W, METAL FILM	R-377-46.4K
R331,341	RES, 220, 5%, 125MW, METAL FILM (1206)	R-375-220
R332	RES, 100K, 5%, 250MW, METAL FILM(1210)	R-376-100K
R334	RES, 23.2K, 1%, 1/8W METAL FILM	R-377-23.2K
R335	RES, 2.274K, .1%, 1/10W, METALFILM	R-263-2.274K
R340,386	RES, 150, 5%, 125MW, METAL FILM (1206)	R-375-150
R342	RES, 90K, .1%, 1/10W, METAL FILM	R-263-90K
R343	RES,10K,.1%,1/10W, METAL FILM	R-263-10K
R344	RES NET, 900,90,9, 10%	TF-168-1
R348	RES, 82K, 5%, 125MW, METAL FILM(1206)	R-375-82K
R349	RES, 2.7K, 5%, 125mW, METAL FILM (1206)	R-375-2.7K
R350	RES, 41.2K, 1%, 125mW, METAL FILM (1206)	R-391-41.2K
R353	RES, 182, 1%, 125MW, METAL FILM (1206)	R-391-182
R354	RES, 100M, 1%, 1/2W, THICK FILM	R-408-100M
R356	RES,750,.5%,3W,METAL FOIL	R-422-750
R358	RES,7.15K, .1%, .2W, WIREWOUND	R-406-7.15K
R359,362	RES, 13K, 5%,125MW, METAL FILM(1206)	R-375-13K
R363,387	RES, 10K, 5%, 6.5W, WIREWOUND	R-336-10K
R364,373	RES, 200K, 5%, 250MW, METAL FILM (1210)	R-376-200K

Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
R365	RES, 78.7K, .1%, .2W, WIREWOUND	R-406-78.7K
R366	RES,1M,0.1%,1/4W,METAL FILM	R-433-1M
R367	RES,22M,5%,1/4W,COMPOSITION OR FILM	R-76-22M
R368	RES, 4.99K, 1%, 125mW,METAL FILM (1206)	R-391-4.99K
R369	RES, 36, 5%, 250MW, METAL FILM(1210)	R-376-36
R370,382	RES, 10K, 5%, 250MW, METAL FILM(1210)	R-376-10K
R371	RES, 3.3K 5%, 125MW METAL FILM (1206)	R-375-3.3K
R372,392	RES,2.2M,10%,1/2W, COMPOSITION	R-1-2.2M
R375	RES, 2.2,5%, 125MW, METAL FILM(1206)	R-403-2.2
R377	RES, 68, 5%, 125MW, METAL FILM(1206)	R-375-68
R379,380	RES, 1M, 5%, 125MW, METAL FILM (1206)	R-375-1M
R381	RES, 100, 5%, 125MW, METAL FILM (1206)	R-375-100
R384	RES, 68K, 5%, 125MW METAL FILM (1206)	R-375-68K
R385,396	RES, 510, 5%, 250MW, METAL FILM(1210)	R-376-510
R394	RES NET, 100K, 9.9M, METAL FILM	TF-251
R398	RES, 1K, .1%, 1W, WIREWOUND	R-249-1
R399	RES, 150, 10%, 1W, METAL FILM	R-411-150
R400	RES, 150, 10%, 1/2W, METAL FILM	R-411-150
R401	RES, 500, 1%, 1/2W, METAL FILM	R-411-500
R402,404	RES, 2.15K, 1%, 125MW, METAL FILM(1206)	R-391-2.15K
R403,424	RES, 100K, 5%, 250MW, METAL FILM(1210)	R-376-100K
R408,409	RES, 1.5K, 5%, 250MW, METAL FILM(1210)	R-376-1.5K
R410,411	RES, 470,5%, 125MW, METAL FILM(1206)	R-375-470
R413,422,423,425,426,428	RES, 100K, 5%, 125mW, METAL FILM (1206)	R-375-100K
R414,421	RES,100K,1%,125mW,METAL FILM(1206)	R-391-100K
R415,419,420	RES, 200K, 5%, 250MW, METAL FILM (1210)	R-376-200K
R416-418	RES, 68K, 5%, 125MW METAL FILM (1206)	R-375-68K
R427	RES, 2K, 5%, 125MW, METAL FILM(1206)	R-375-2K
R429	RES, 1M, 5%, 125MW, METAL FILM (1206)	R-375-1M
R432-441,443	RES,1K,5%,125MW,METAL FILM(1206)	R-375-1K
R442	RES, 330, 5%, 125MW, METAL FILM(1206)	R-375-330
R444	RES, 39K, 5%, 250mW, METAL FILM (1210)	R-376-39K
R446,445	RES,4.7K,5%,125MW,METAL FILM(1206)	R-375-4.7K
R447-R449	RES,10K,5%,125MW,METAL FILM(1206)	R-375-10K
R501,560	RES,10K,1%,125mW,METAL FILM(1206)	R-391-10K
R503	RES, 150K, 5%, 125MW, METAL FILM (1206)	R-375-150K
R504,582,536	RES, 33K, 5%, 125MW, METAL FILM(1206)	R-375-33K
R505,512,517,570,571,577	RES, 1M, 5%, 125MW, METAL FILM (1206)	R-375-1M
R506,566,537	RES, 15K, 1%, 125mW, METAL FILM (1206)	R-391-15K
R507	RES,4.7K,5%,125MW,METAL FILM(1206)	R-375-4.7K
R513	RES, 10M, 5%, 125MW, METAL FILM(1206)	R-375-10M
R514	RES, 470,5%, 125MW, METAL FILM(1206)	R-375-470
R515,521	RES, 22K, 5%, 125MW, METAL FILM(1206)	R-375-22K
R516	RES, 120K, 5%, 250mW, METAL FILM (1210)	R-376-120K
R520	RES, 330, 5%, 125MW, METAL FILM(1206)	R-375-330
R522	RES, 2.15K, 1%, 125MW, METAL FILM(1206)	R-391-2.15K
R526	RES, 100, 5%, 125MW, METAL FILM (1206)	R-375-100

Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
R527,535,565	RES,7.5K,5%,125MW,METAL FILM(1206)	R-375-7.5K
R530	RES NET,250K,9.34K,1K,10.233K,15K,7K	TF-226
R531	RES NET, 1K,1K	TF-227
R533	RES, 4.99K, 1%, 125mW,METAL FILM (1206)	R-391-4.99K
R538,540,545	RES,10K,5%,125MW,METAL FILM(1206)	R-375-10K
R541	RES,49.9K,1%,125MW, METAL FILM (1206)	R-391-49.9K
R542	RES, 1K, 1%, 125mW, METAL FILM (1206)	R-391-1K
R544	RES, 100K, 1%, 125mW, METAL FILM (1206)	R-391-100K
R546,561,580	RES, 6.65K, 1%, 125MW, METAL FILM(1206)	R-391-6.65K
R548,549	RES, 1K,1%,1/2W FUSIBLE METAL FILM	R-370-1K
R550,R556	RES, 499K, 1%, 125MW, METAL FILM(1206)	R-391-499K
R551	RES, 90.9K, 1%, 125mW, METAL FILM (1206)	R-391-90.9K
R554,555	RES, 68K, 5%, 125MW METAL FILM (1206)	R-375-68K
R557	RES NET, 1100K@.990W,11.111K@.010W,1%	TF-225
R558	RES, 49.9, 1%, 125mW, METAL FILM (1206)	R-391-49.9
R559	RES, 11K, 5%,250MW,METAL FILM(1210)	R-376-11K
R562	RES,100K,5%,1/4W,COMPOSITION OR FILM	R-76-100K
R563	RES, 2.74K, .1%, 1/10W, METAL FILM	R-263-2.74K
R573	RES, 3.3K 5%, 125MW METAL FILM (1206)	R-375-3.3K
R575,576	RES, 487K, 1%, 125mW, METAL FILM (1206)	R-391-487K
R581	RES, 33, 5%, 250mW, METAL FILM (1210)	R-376-33
R583	RES, 100K, 5%, 250MW, METAL FILM(1210)	R-376-100K
R584	RES, 1M, 5%, 250MW METAL FILM (1210)	R-376-1M
R585,593	RES, 200K, 5%, 250MW, METAL FILM (1210)	R-376-200K
R591	RES, .1, 1%, 2W, 4-TERMINAL MOLDED	R-342-.1
R592	RES, .91, .1, 1/4W WIREWOUND	R-95-.91
R596,597	RES, 2K, 5%, 125MW, METAL FILM(1206)	R-375-2K
R599	RES,10K,5%,125MW,METAL FILM(1206)	R-375-10K
R600	RES,330,5%,125MW,METAL FILM (1206)	R-375-330
R601	RES,1.2M,5%,125MW,METAL FILM (1206)	R-375-200K
R602	RES,200K,5%,125MW,METAL FILM (1206)	R-375-1.2M
S100	SWITCH,PUSHBUTTON (6 POLE)	SW-466
S300	SWITCH, PUSHBUTTON, 8 POLE	SW-468
U100	IC, MOSFET DRIVER, TLP590A	IC-812
U102	IC,NEG VOLTAGE REG -15V,500MA,79M15	IC-195
U103	IC,VOLTAGE REGULATOR,LM317T	IC-317
U105,109	IC, OPTO-COUPLER, HIGH EMI, H11AV1A	IC-845
U106	IC, VOLT. COMPARATOR,LM311M (SOIC)	IC-776
U107	IC,POS VOLTAGE REG +15V,500MA,7815	IC-194
U108	IC,+5V VOLTAGE REGULATOR,LM2940CT	IC-576
U110	IC, TIMING CIRCUIT, MC1455D (SOIC)	IC-847
U300,302,303,305,307	IC, 8 STAGE SHIFT/STORE,MC14094BD(SOIC)	IC-772
U301	IC, DUAL D-TYPE F/F, 74HC74(SOIC)	IC-773

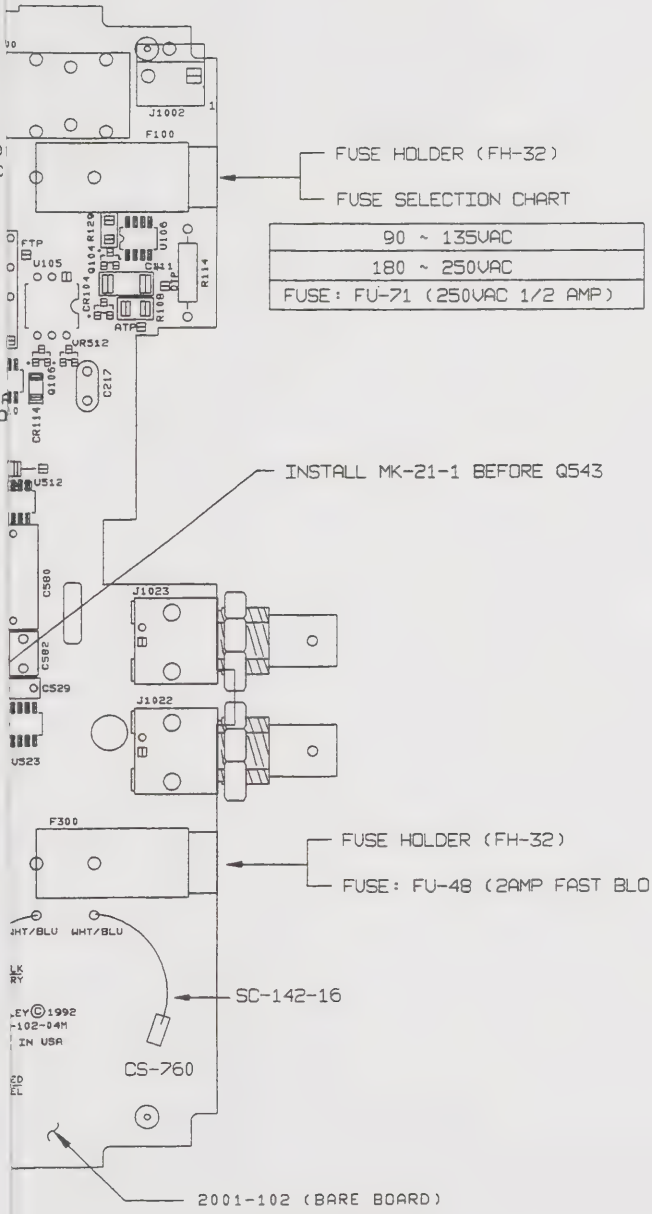
Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
U304,306,309,310,316	IC, QUAD COMPARATOR,LM339D (SOIC)	IC-774
U308,334	IC, TRI-2CH MULTI/DEMUX, 4053 (SOIC)	IC-770
U311-315	IC,OPTOCOUPLER,TLP582	IC-689
U317	IC, CMOS ANAL. SWITCH, DG411DY(SOIC)	IC-785
U318-320,323	IC,CMOS ANALOG SWITCH DG211DY(SOIC)	IC-768
U321	IC, HEX LEVEL SHIFTER, MC14504B (SOIC)	IC-771
U322	IC,22V OP-AMP, LT1007ACN8	IC-422
U324,328	IC,OP-AMP,AD707,(SOIC)	IC-712
U325,332	IC, SELECTED IC-739, MC14052B	2001-600A
U327	IC, OP-AMP, LTC1050CS8(SOIC)	IC-791
U329	IC, PRECISION REFERENCE, LM399	196-600A
U330	IC,SWITCHING CAP BLOCK, LTC1043CN	IC-745
U331	IC, OP-AMP, LF351M(SOIC)	IC-815
U333	IC, OP-AMP, AD705JR(SOIC)	IC-814
U335	IC, OP-AMP, LT1007CN8	IC-744
U336-339	IC, TLP591B	IC-877
U340	IC, VOLT COMPARATOR LM393D(SOIC)	IC-775
U341	IC, BIFET OP-AMP, AD548 (SOIC)	IC-876
U342	IC, 20V OP-AMP, LT1097S8 (SOIC)	IC-767
U500,501,505,530	IC, 8 STAGE SHIFT/STORE,MC14094BD(SOIC)	IC-772
U502	IC, -5V REGULATOR, 79L05ACM (SOIC)	IC-787
U503	IC, RETRIG., MULTIVIB, 74HC123AM (SOIC)	IC-788
U506	IC, VOLT COMPARATOR LM393D(SOIC)	IC-775
U507	IC, VOLT. COMPARATOR, LT1016CS8(SOIC)	IC-797
U508,513,536	IC, QUAD 2-INPUT NAND, 74HC00M (SOIC)	IC-781
U509	IC, MCHAN LAT DMOS QUAD FET, SD5400CY (SOIC)	IC-893
U510,U515,532	IC,CMOS ANALOG SWITCH DG211DY(SOIC)	IC-768
U511	IC, 8-CHAN ANA MULTIPLEXER,DG408DY(SOIC)	IC-844
U512	IC, VOLT. COMPARATOR,LM311M (SOIC)	IC-776
U514,529	IC, OP-AMP, AD847JR (SOIC)	IC-779
U516,519	IC,OP-AMP, AD848JR (SOIC)	IC-784
U517	IC,TRMS TO DC CONVERTER, 637JR (SOLIC)	IC-796
U518,537	IC,MOSFET DRIVER, TLP590A	IC-812
U520	IC, OP-AMP LT1223C58(SOIC)	IC-873
U521,524	IC, 20V OP-AMP, LT1097S8 (SOIC)	IC-767
U522	IC, CMOS ANAL. SWITCH, DG411DY(SOIC)	IC-785
U523	IC, DUAL OP-AMP, LF353M (SOIC)	IC-842
U525	IC, OP-AMP, LTC1050CS8(SOIC)	IC-791
U526	IC, CMOS ANAL SWITCH, DG444DY, (SOIC)	IC-866
U527	IC, QUAD COMPARATOR,LM339D (SOIC)	IC-774
U528	IC, DUAL OP-AMP, 1458 (SOIC)	IC-811
U531	IC, DUAL 8-BIT DAC, MP7528JS(SOIC)	IC-810
U533	IC, SUPPLY VOLT SUPERVISOR,TL7705A(S0IC)	IC-860
U534	IC, OP-AMP, BIFET, AD548(SOIC)	IC-894
U535	IC, MOSFET DRIVER, TSC428CBA (SOIC)	IC-872
U538	IC,TLP591B	IC-877

Table 4-2 (continued)
Model 2001 analog board, parts list

Circuit Desig.	Description	Keithley Part No.
VR100	DIODE, ZENER 22V, BZX84C22 (SOT-23)	DZ-86
VR101	DIODE, ZENER 6.2V, BZX84B6V2 (SOT-23)	DZ-87
VR102	DIODE, ZENER, 39V, MLL4716(MLL-34)	DZ-95
VR300,304	DIODE,ZENER 5.1V, BZX84C5V1 (SOT-23)	DZ-88
VR302,307	DIODE,ZENER 6.44V,IN4577AGED (DO-7)	DZ-58
VR305,306	DIODE, ZENER, 22V, BZV55C22 (SOD-80)	DZ-96
VR308,309	DIODE, ZENER 15V, IN5352 (CASE 17)	DZ-76
VR310,311	DIODE, ZENER 6.2V, BZX84B6V2 (SOT-23)	DZ-87
VR502	DIODE, ZENER, 8.2V, MMBZ5237 (SOT-23)	DZ-92
VR503,505	DIODE,ZENER 15V,1N4744A (TO-41)	DZ-75
VR504,507,508	DIODE, ZENER, 4.3V,BZX84C4V3 (SOT-23)	DZ-85
VR506,509	DIODE,ZENER 5.1V, BZX84C5V1 (SOT-23)	DZ-88
VR510,511	DIODE, ZENER 3.3V, MMBZ5226BL(SOT-23)	DZ-94
VR512	DIODE, ZENER 6.2V, BZX84B6V2 (SOT-23)	DZ-87
VR513	DIODE ZENER, 10V, IN5240C(DO-35)	DZ-93
W100	JUMPER	J-15

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911114	RELEASED		
F	14931	REVISED		
GKAR		PRELIMINARY		
H	15229	REVISED		4/21/92
H1	15270	REVISED TO ADD NOTE •		4/29/92
J	15292	REVISED,ADDED CR538 & CR539	SZ	5/15/92
J1	15317	SEE PAGE 2	SZ	6/10/92
J2	15228	SEE PAGE 2	AS	6/23/92
K	15365	ARTWORK WAS REV J. ADDED Q548,Q549,R219 AND R290. DELETED CR329,CR330,R207 AND R208.	AS	8/11/92
L	15521	ARTWORK WAS REV K. ADDED Q341 & Q342. DELETED R291 & R401. CHG'D VALUES OF C563,Q304 Q306,R290,R308,R421,U509 & U534. RELOCATED PARTS FROM BOTTOM TO TOP SIDE OF BOARD.	AS	1/8/93
M	16440	ARTWORK WAS REV.L	SZ	4/19/94
M1	17108	ADDED MK-21-1 TO Q543		8-7-94



MODEL	NEXT ASSEMBLY	QTY.
	USED ON	

RANCES PECIFIED	DATE 7/9/92	SCALE 5:4	TITLE COMPONENT LAYOUT ANALOG BOARD
ANG. ±1°	DRN. CB	ENG. APPR.	
RC. ±1/64	MATERIAL	C	NO. 2001-100
	FINISH		

ORIGINAL ISSUED 1 OF 2

NO. 2001-100

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911114	RELEASED		
F	14931	REVISED		
GKAR		PRELIMINARY		
H	15229	REVISED		4/21/92
H1	15270	REVISED TO ADD NOTE *		4/29/92
J	15292	REVISED,ADDED CR538 & CR539	SZ	5/15/92
J1	15317	SEE PAGE 2	SZ	6/10/92
J2	15228	SEE PAGE 2	AS	6/23/92
K	15365	ARTWORK WAS REV J. ADDED Q548,Q549,R219 AND R290. DELETED CR329,CR330,R267 AND R288.	AS	8/11/92
L	15521	ARTWORK WAS REV K. ADDED Q541 & Q342. DELETED R291 & R401. CHG'D VALUES OF C563,Q304 Q306,R290,R398,R421,U509 & U534. RELOCATED PARTS FROM BOTTOM TO TOP SIDE OF BOARD.	AS	1/8/93
M	16440	ARTWORK WAS REV.L	SZ	4/19/94
M1	17108	ADDED MK-21-1 TO Q543		8/1/94

COMPONENT SIDE VIEW

CA-27-16C

J1026
CONNECTOR (CS-765)

STANDOFF (ST-202-1)
3 REQ'D

MK-21-1
(3 REQ'D)

PRINTED FLAT EDGE TO OUTSIDE

2001-162
(ADC BOARD)

HS-41
5 REQ'D

INSTALL R592 BEFORE R591

FUSE HOLDER (FH-32)

FUSE SELECTION CHART

90 ~ 135VAC
180 ~ 250VAC
FUSE: FU-71 (250VAC 1/2 AMP)

INSTALL L100
BEFORE C316

INSTALL MK-21-1 BEFORE Q543

FUSE HOLDER (FH-32)

FUSE: FU-48 (2AMP FAST BLO)

SC-142-16

CS-760

2001-102 (BARE BOARD)

SC-142-16

TX-17-1/4x5/16,SHRINK TUBING

SP-5

WHT | BLK | GREY | YEL | RED
WHT/BLU | WHT/BLK | WHT/GRY | WHT/YEL | WHT/RED

SC-142-0 & CS-760
SC-142-10 & CS-760
SC-142-8 & CS-760
SC-142-18 & CS-760
SC-142-4 & CS-760
SC-142-14 & CS-760
SC-142-2 & CS-760
SC-142-12 & CS-760

SC-142-* WIRES:
REFER TO PRODUCT STRUCTURE
FOR COMPLETE INFORMATION.

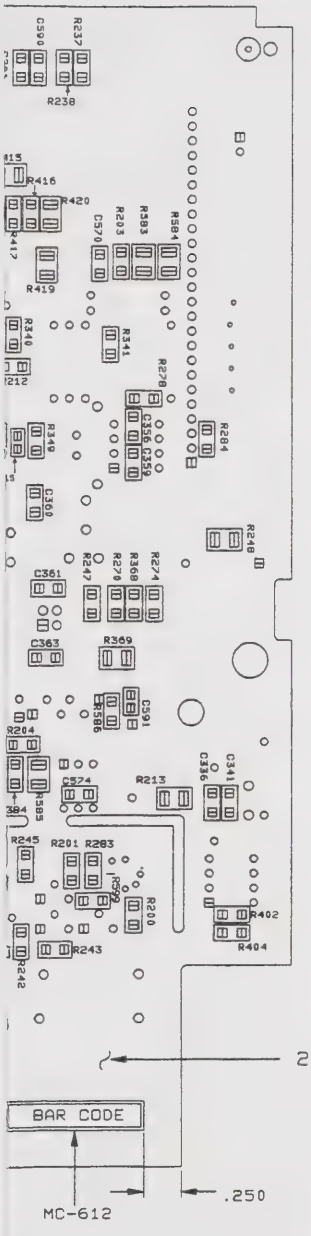
*NOTE: DO NOT INSTALL

MODEL	NEXT ASSEMBLY	QTY.
	USED ON	

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 7/9/92	SCALE 5:4	TITLE COMPONENT LAYOUT ANALOG BOARD
KEITHLEY KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. CB	ENG. APPR.	
	XXX=±.005 FRAC.=±1/64	MATERIAL	C	NO. 2001-100
	SURFACE MAX. 63	FINISH		

ORIGINAL ISSUED 1 OF 2

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911112	RELEASED		
F	14931	REVISED		
GKAR		PRELIMINARY		
H	15229	REVISED		4/13/92
H1	15270	REVISED PAGE 1		4/29/92
J	15292	REVISED	SZ	5/15/92
J1	15317	REVISED, LOCATED MC-612	SZ	6/10/92
J2	15228	DEL "DO NOT INSTALL" NOTE FOR CR526..CR528	AS	6/23/92
K	15365	ARTWORK WAS REV J. ADDED R292. DELETED C349 AND C354. CHG'D VALUES OF R239,R385 & R386.	AS	8/11/92
L	15521	ARTWORK WAS REV K. DEL C200,C355,C400 & C598 CHG'D VALUES OF R210,R263,R264,R308,R309 AND R316-R319. RELOCATED PARTS FROM BOT TO TOP.	SZ	1/8/93
M	16440	ARTWORK WAS REV.L	SZ	4/19/94
M1	17108	REVISED SEE PAGE 1		



MODEL	NEXT ASSEMBLY USED ON	QTY.

RANCES SPECIFIED	DATE 7/9/92	SCALE 5:4	TITLE COMPONENT LAYOUT ANALOG BOARD
ANG.=±1°	DRN. CB	ENG. APPR.	
AC.=±1/64	MATERIAL	C	NO. 2001-100
3	FINISH		

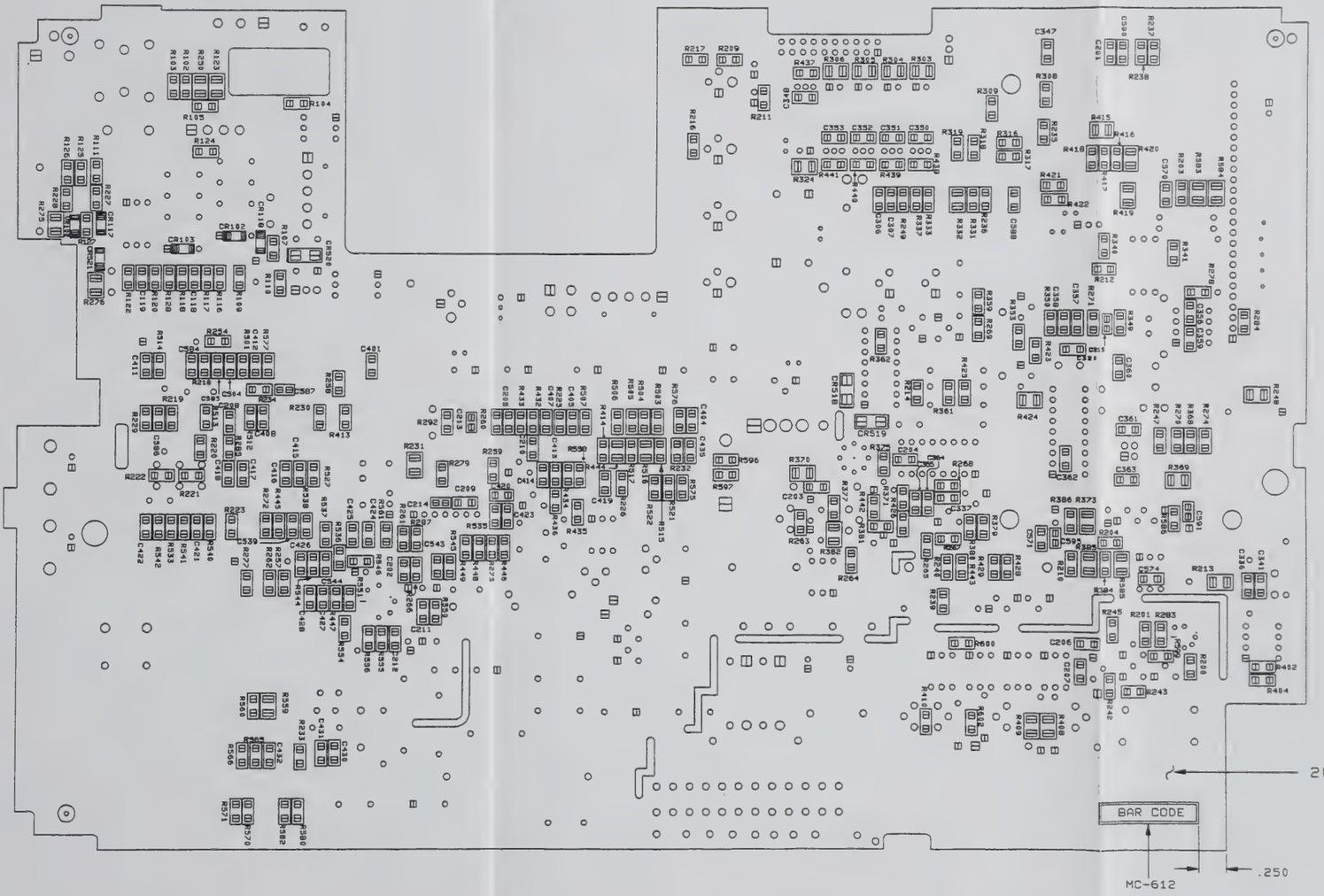
ORIGINAL IF RED

U-16B

NO. 2001-100

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911112	RELEASED		
F	14931	REVISED		
GKAR		PRELIMINARY		
H	15229	REVISED		4/13/92
H1	15270	REVISED PAGE 1		4/29/92
J	15292	REVISED	SZ	5/15/92
J1	15317	REVISED, LOCATED MC-612	SZ	6/10/92
J2	15228	DEL "DO NOT INSTALL" NOTE FOR CR526..CR528	AS	6/23/92
K	15365	ARTWORK WAS REV J. ADDED R292. DELETED C349 AND C354. CHG'D VALUES OF R239,R385 & R386.	AS	8/11/92
L	15521	ARTWORK WAS REV K. DEL C200,C355,C400 & C500 CHG'D VALUES OF R210,R263,R264,R308,R309 AND R316-R319. RELOCATED PARTS FROM BOT TO TOP.	SZ	1/8/93
M	16440	ARTWORK WAS REV.L	SZ	4/19/94
M1	17108	REVISED SEE PAGE 1		

SOLDER SIDE VIEW



2001-102 (BARE BOARD)

BAR CODE

MC-612

.250

MODEL	NEXT ASSEMBLY	QTY.
	USED ON	

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 7/9/92	SCALE 5:4
KEITHLEY KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. CB	ENG. APPR.
	XXX=±.005 FRAC.=±1/64	MATERIAL	
	SURFACE MAX. 63	FINISH	

TITLE COMPONENT LAYOUT ANALOG BOARD

C NO. 2001-100

G PG 2 OF 2

ORIGINAL IF RED

4-186 B

Table 4-3
Model 2001 digital board, parts list

Circuit Desig.	Description	Keithley Part No.
	CONN,BERG	CS-339
	SOCKET (USE WITH U608)	SO-134-32
	SOCKET, 44 PIN QUAD (USE WITH U611)	SO-128-44
C101	CAP,1,20%,250V,ALUMINUM ELECTROLYTIC	C-400-1
C102	CAP,10UF,20%,25V,TANTALUM (D7243)	C-440-10
C602-607,620,636-640,661, 665-667,C670	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
C609	CAP, .1UF, 20%,100V, CERAMIC (1812)	C-436-.1
C611	CAP, 15000uF, 20%, 16V, ALUM ELECT.	C-450-15000
C613,619,632	CAP, 10UF,20%, 25V, TANTALUM (D7243)	C-440-10
C617,618	CAP, 33PF, 10%, 100V, CERAMIC (1206)	C-451-33P
C621-623,626-628,664,668	CAP, .01uF, 20%, 50V, CERAMIC (1206)	C-418-.01
C624,630,633	CAP, 1000UF, +/-20%, 16V, ALUMINUM	C-488-1000
C625	CAP, 47UF,10%,16V,ALUM ELEC	C-321-47
C631	CAP, 3.3UF, 20%, 50V, POLY-FILM	C-470-3.3
C641-659,671,672	CAP,270PF,20%,100V,CERAMIC/FERRITE	C-386-270P
C668	CAP, .01uF, 20%, 50V, CERAMIC (1206)	C-418-.01
C669	CAP, 47PF, 10%, 100V, CERAMIC(1206)	C-451-47P
CR101,102	DIODE,SWITCHING,MMBD914(SOT-23)	RF-83
CR103-106	DIODE,SWITCHING,250MA,BAV103 (SOD-80)	RF-89
CR602-619,626	DIODE, SWITCHING, 250MA,BAV103 (SOD-80)	RF-89
CR622	DIODE, BRIDGE PE05 (CASE KBU)	RF-48
CR624,625	DIODE,SILICON,IN4006 (D0-41)	RF-38
CR627,628	DIODE,ARRAY,MMAD1103,(SOIC)	RF-80
J1027	CONN,HEADER STRAIGHT SOLDER PIN	CS-368-20
J1028	CONN,RIGHT ANGLE,24PIN	CS-507
J1029,1030	CONN, MICRODIN W/GND FINGERS	CS-792
J1031	CONN, RT ANGLE, MALE, 9 PIN	CS-761-9
J1032	CONN, RT. ANGLE, MALE MOLEX .156	CS-715-4
J1033	CONN, HEADER STRAIGHT SOLDER PIN	CS-368-16
J1034	CONN, MALE RT ANGLE, 32-PIN	CS-456
J1037	FOR FN-26 CONN, MALE 3 PIN	CS-612-1
L603-607	CHOKE, SHIELD BEAD	CH-52

Table 4-3 (continued)
Model 2001 digital board, parts list

Circuit Desig.	Description	Keithley Part No.
Q101,102	TRANS,NPN	TG-271
Q602-607	TRANS,N CHAN MOSPOW FET,2N7000 (TO-92)	TG-195
Q608	TRANS,N-CHANNEL FET,TN06L TG-216	TG-216
R101	RES,240,250MW,METAL FILM(1210)	R-376-240
R102	RES,1K,250MW,METAL FILM(1210)	R-376-1K
R103	RES,1M,125MW,METAL FILM(1210)	R-375-1M
R601,603-605,610,R672	RES, 2K, 1%, 125mW, METAL FILM (1206)	R-391-2K
R606,607	RES, 4.7K, 5%, 250MW, METAL FILM(1210)	R-376-4.7K
R616,621,625,629,R631	RES,10,5%,125MW,METAL FILM(1206)	R-375-10
R639	RES, 680K, 5%,125mW, METAL FILM (1206)	R-375-680K
R644	RES NET,4.7K,2%,1.875W(SOMIC)	TF-219-4.7K
R648-650,655-657	RES, 5.1K,5%, 125MW, METAL FILM (1206)	R-375-5.1K
R663,677	RES,4.7K,5%,125MW,METAL FILM(1206)	R-375-4.7K
R665	RES, 470,5%, 125MW, METAL FILM(1206)	R-375-470
R667,669	RES, 560, 5%, 250mW, METAL FILM (1210)	R-376-560
R668	RES, 10K, 5%, 250MW, METAL FILM(1210)	R-376-10K
R670,675	RES,100,5%,250MW,METAL FILM(1210)	R-376-100
R705	RES, 15K, 1%, 125mW, METAL FILM (1206)	R-391-15K
R706,708,711,729	RES, 10K, 1%, 125mW, METAL FILM (1206)	R-391-10K
R707	RES, 150, 5%, 250MW, METAL FILM (1210)	R-376-150
R709	RES, 14K, 1%, 125mW, METAL FILM (1206)	R-391-14K
R710,716	RES, 1M, 5%, 250MW METAL FILM (1210)	R-376-1M
R712	RES, 100K, 1%, 125mW, METAL FILM (1206)	R-391-100K
R713	RES, 200K, 1%, 125MW, METAL FILM (1206)	R-391-200K
R714	RES, 4.7K, 5%, 250MW, METAL FILM(1210)	R-376-4.7K
R715,743-748,752-755,757, 768-770	RES, 100, 5%, 125MW, METAL FILM (1206)	R-375-100
R717,720	RES, 10K, 5%, 250MW, METAL FILM(1210)	R-376-10K
R718,719,730	RES,1K, 5% 250MW, METAL FILM (1210)	R-376-1K
R721	RES, 2.15K, 5%, 250MW, METAL FILM (1210)	R-376-2.15K
R732-742,749,771	RES,10K,5%,125MW,METAL FILM(1206)	R-375-10K
R758-763	RES, 39, 5%, 125MW, METAL FILM(1206)	R-375-39
R772	RES,47K,5%,125MW,METAL FILM(1206)	R-375-47K
T101	TRANSFORMER	TR-292A
TP601-603	CONN,TEST POINT	CS-553

Table 4-3 (continued)
Model 2001 digital board, parts list

Circuit Desig.	Description	Keithley Part No.
U608	IC,(8KX8)HI SPEED STATIC CMOS RAM,6264	LSI-66
U609,610,635,636	IC,32KX8 STAT CMOS RAM,D43256C(SOMETRIC)	LSI-93-100
U611	PROGRAM	2001-800-**
U612	IC,350MA SATURATED SINK DRIVER UDN-2596A	IC-578
U614	IC,OCT BFR/LINE DRIVE,74HCT244(SOLIC)	IC-651
U615,630	IC, QUAD 2 IN NOR, 74HCT02 (SOIC)	IC-809
U616	IC, QUAD 2 INPUT OR, 74HCT32 (SOIC)	IC-808
U617	IC, SERIAL E EPROM, X24C16(8-PIN DIP)	IC-736
U618	PROGRAM	2001-801-**
U619,629	IC,+5V VOLTAGE REGULATOR,LM2940CT	IC-576
U620	IC, DUAL POWER-SUPPLY SUPER, TL7770-5	IC-805
U621	IC,OCTAL INTERFACE BUS,75160(SOLIC)	IC-646
U622	IC, GPIB ADAPTER, 9914A (PLCC)	LSI-123
U623	IC,OCTAL INTER BUS TRANS,75161(SOLIC)	IC-647
U625	MOD,DC-AC/DC, 5DV-5VAC/60DC,E705-E905VF,MO-30	182-170B
U626	IC, 16-BIT MICRO, MC68302FE	LSI-106
U627	IC, 18V OP-AMP, TLC 271	IC-347
U628	IC, VOLT COMPARATOR LM393D(SOIC)	IC-775
U631	IC,16-BIT MICRO,MC68302FC	LSI-144
U634	IC,SERIAL EEPROM, X24164(8-PIN DIP)	IC-885
U637	PROGRAM	2001-803-**
U638	PROGRAM	2001-804-**
VR601	DIODE, ZENER, 8.2V, MMBZ5237 (SOT-23)	DZ-92
VR602,603	DIODE,ZENER,4.7V,IN4732A(D0-41)	DZ-67
W602,603	JUMPER	J-15
W605,606	CONN,3 PIN	CS-339-3
W606	CONNECTOR, JUMPER	CS-476
Y602	CRYSTAL, 16MHZ	CR-30-16M
Y603	OSCILLATOR CMOS 4,MHZ(SMT)	CR-34

** Order present firmware revision level for main CPU (i.e., 2001-801-A05).

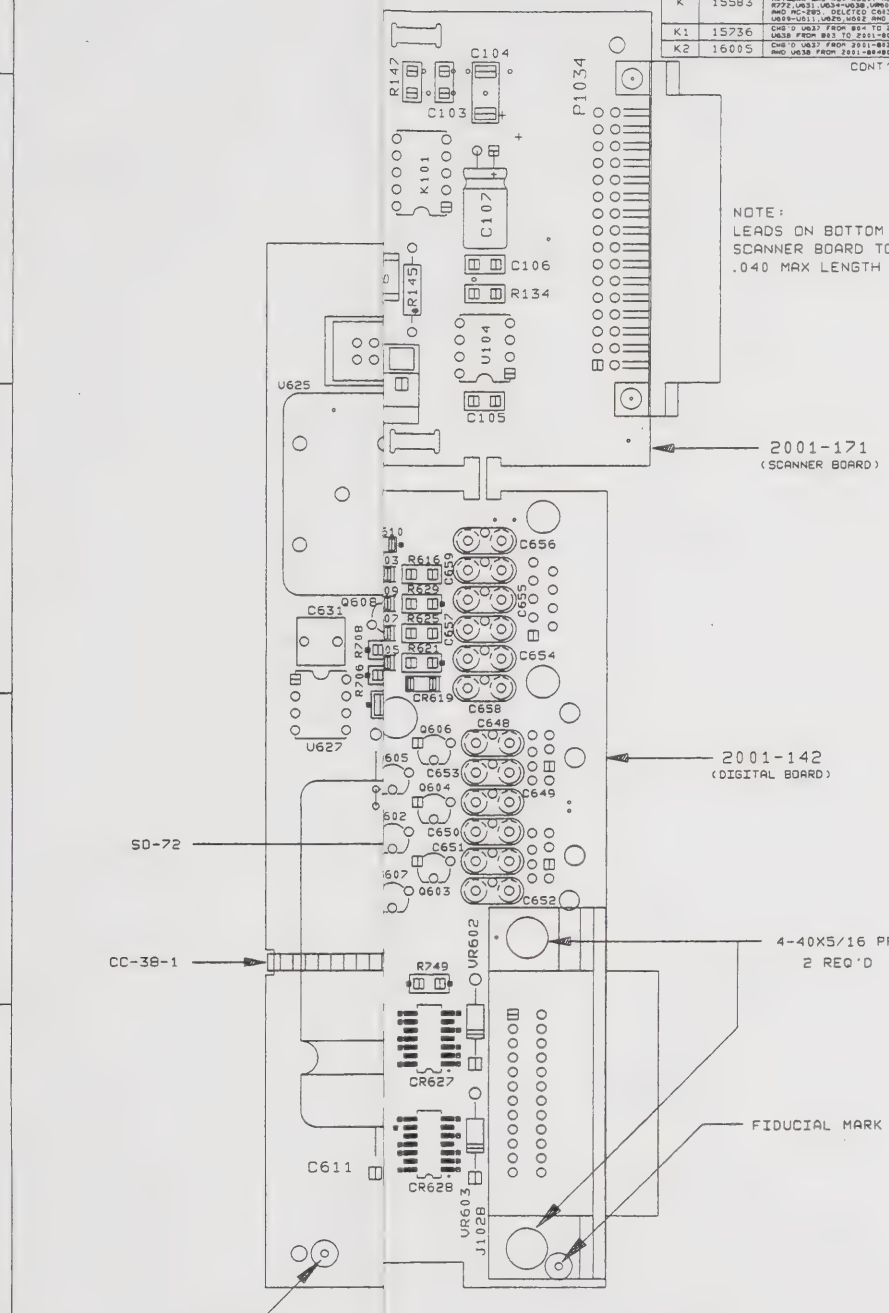
2001-140-170
NO.

NER BOARD) REVISION CONTROL		
REVISION	ENG.	DATE
SED	MS	10/15/91
D	SZ	11/20/91
MC-612 BAR CODE LABEL LEAD TRIMMING NOTE	SZ	1/2/92
D	SZ	2/25/92
D MC-612A BAR CODE LABEL		

2001-140 (DIGITAL BOARD) REVISION CONTROL				
LTR.	ECO NO.	REVISION	ENG.	DATE
E	911015	RELEASED	MS	10/15/91
F	14917	REVISED	SZ	11/20/91
F1	15012	RELOCATED MC-612 BAR CODE LABEL	SZ	1/2/92
G	15042	REVISED	MS	1/11/92
H	15066	REVISED	SZ	2/25/92
J	15329	CHG'D ARTWORK FROM REV H TO J.	AS	6/5/92
J1	15473	ADDED 2001-880A03 UNDER U611 AND 2001-881A13 UNDER U618.	SZ	10/2/92
J2	15524	CHG'D 2001-880A05 TO 2001-880A06(U611)	SZ	11/12/92
KDEV		ARTWORK WAS REV J.		
K	15583	ARTWORK WAS REV KDEV. ADDED C671,C672,R771, R772,U631,U634=U638,U8902,U8903,(2)150-134-32 AND MC-2B5. DELETED C613,R736,SO-128-44, U639-U811,U8270,U8912 AND U803.	AS	1/12/93
K1	15736	CHG'D U637 FROM 804 TO 2001-883802 AND U638 FROM 803 TO 2001-883802	AS	3/4/93
K2	16005	CHG'D U637 FROM 2001-883802 TO 2001-883805 AND U638 FROM 2001-884802 TO 2001-884803.	SZ	8/2/93

CONT'D.

NOTE:
LEADS ON BOTTOM SIDE OF 2001-172 SCANNER BOARD TO BE TRIMMED TO .040 MAX LENGTH AFTER FLOW SOLDER.



ORE COMPONENT INFORMATION REFER
01 PRODUCT STRUCTURE.

2001		
MODEL	NEXT ASSEMBLY	QTY.
USED ON		

AWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 10/15/91	SCALE 2:1	TITLE COMPONENT LAYOUT, DIGITAL BOARD & SCANNER BOARD
	XX=±.015 ANG.=±1°	DRN. MAH	ENG. APPR.	
MENTS INC. 44139	XXX=±.005 FRAC.=±1/64	MATERIAL		D NO. 2001-140-170
	SURFACE MAX. 63	FINISH		

ORIGINAL W [illegible] H PG.1 OF 2

4-180

NO. 2001-140-170

2001-140 (DIGITAL BOARD) REVISION CONTROL

LTR.	ECO NO.	REVISION	ENG.	DATE
K3	16057	ADDED SO-72	S2	9/27/93
K4	16150	CHG'D U637 FROM 2001-B03895 TO 2001-B03896 AND U638 FROM 2001-B04823 TO 2001-B04824.	S2	10/29/93
K5	16409	CHG'D U637 FROM 2001-B03896 TO 2001-B03897 AND U638 FROM 2001-B04824 TO 2001-B04825.	S2	3/14/94
K6	16766	CHG'D U637 FROM 2001-B03897 TO 2001-B03898 AND U638 FROM 2001-B04825 TO 2001-B04826.	S2	10/10/94
K7	17540	CHG'D U637 FROM 2001-B03898 TO 2001-B03899 AND U638 FROM 2001-B04826 TO 2001-B04827.	S2	7/27/95

2001-170 (SCANNER BOARD) REVISION CONTROL

LTR.	ECO NO.	REVISION	ENG.	DATE
D	911015	RELEASED	MS	10/15/91
E	14912	REVISED	S2	11/20/91
E1	15012	ADDED MC-612 BAR CODE LABEL ADDED -EAD TRIMMING NOTE	S2	1/2/92
F	15066	REVISED	S2	2/25/92
F1	17051	REMOVED MC-612A BAR CODE LABEL		

2001-140 (DIGITAL BOARD) REVISION CONTROL

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911015	RELEASED	MS	10/15/91
F	14917	REVISED	S2	11/20/91
F1	15012	RELOCATED MC-612 BAR CODE LABEL	S2	1/2/92
G	15042	REVISED	MS	1/11/92
H	15066	REVISED	S2	2/25/92
J	15329	CHG'D ARTWORK FROM REV H TO J.	AS	6/5/92
J1	15473	ADDED 2001-B03893 UNDER U611 AND 2001-B03897 UNDER U613.	S2	10/2/92
J2	15524	CHG'D 2001-B03A05 TO 2001-B03A06(U611)	S2	11/12/92
KDEV		ARTWORK WAS REV J.		
K	15593	ARTWORK WAS REV. K. ECO: ADDED C671,C672,R771, R772,U631,U634-U636,U6852,U6853,(2)EPROM-15-32 AND MC-292. DELETES C613,R750,50-129-00, U629-U631,U635,U637 AND U651.	AS	1/12/93
K1	15736	CHG'D U637 FROM 897-TC 2001-B03892 AND U638 FROM 893 TO 2001-B04897.	AS	3/4/93
K2	16005	CHG'D U637 FROM 2001-B03892 TO 2001-B03895 AND U638 FROM 2001-B04827 TO 2001-B04827.	S2	6/2/93

CONT'D.

FIDUCIAL MARK

MC-285, TOP SIDE

*NOTE: DO NOT INSTALL R145, R146

NOTE:
LEADS ON BOTTOM SIDE OF 2001-172 SCANNER BOARD TO BE TRIMMED TO .040 MAX LENGTH AFTER FLOW SOLDER.

2001-171 (SCANNER BOARD)

2001-142 (DIGITAL BOARD)

4-40X5/16 PPH 2 REQ'D

FIDUCIAL MARK

SO-72

CC-38-1

FIDUCIAL MARK

MC-612, TOP SIDE

SO-134-32 3 PLACES

FIDUCIAL MARK

*NOTE: DO NOT INSTALL C673, C674, U632, U633

NOTE: FOR MORE COMPONENT INFORMATION REFER TO 2001 PRODUCT STRUCTURE.

TOP SIDE COMPONENTS

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 10/15/91	SCALE 2:1	TITLE	COMPONENT LAYOUT, DIGITAL BOARD & SCANNER BOARD	
KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. MAW	ENG. APPR.			
	XXX=±.005 FRAC.=±1/64	MATERIAL				
	SURFACE MAX. 63	FINISH		D	NO 2001-140-170	

2001 MODEL | NEXT ASSEMBLY | QTY. USED ON

ORIGINAL PG.1 OF 2

4-180

2001-140-170
NO.

NNER BOARD) REVISION CONTROL		
REVISION	ENG.	DATE
ED	MS	10/15/91
D	SZ	11/20/91
ED MC-612 TO TOP SIDE	SZ	1/2/92
D	SZ	2/25/92
D SEE PG.1		8-14-92

2001-140 (DIGITAL BOARD) REVISION CONTROL

LTR.	ECO NO.	REVISION	ENG.	DATE
E	911015	RELEASED	MS	10/15/91
F	14917	REVISED	SZ	11/20/91
F1	15012	SEE PAGE 1	SZ	1/2/92
G	15042	REVISED	MS	1/11/92
H	15066	REVISED	SZ	2/25/92
J	15329	CHG'D ARTWORK FROM REV H TO J.	AS	6/5/92
J1	15473	SEE PAGE 1	SZ	10/2/92
J2	15524	SEE PAGE 1	SZ	11/12/92
KDEV		ARTWORK WAS REV J.		
K	15583	ARTWORK WAS REV KDEV. ADDED C603	AS	1/12/93
K1	15736	SEE PAGE 1	AS	3/4/93
K2	16005	SEE PAGE 1	SZ	8/2/93
K3	16057	SEE PAGE 1	SZ	9/27/93
K4	16150	SEE PAGE 1	SZ	10/29/93
K5	16409	SEE PAGE 1	SZ	3/14/94
K6	16766	SEE PAGE 1	SZ	10/11/94
K7	17540	SEE PAGE 1	SZ	7/27/95

2001-171
(SCANNER BOARD)

J1029

2001-142
(DIGITAL BOARD)

MORE COMPONENT INFORMATION REFER
001 PRODUCT STRUCTURE.

2001		
MODEL	NEXT ASSEMBLY USED ON	QTY.

RAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 10/15/91	SCALE 2:1	TITLE COMPONENT LAYOUT, DIGITAL BOARD & SCANNER BOARD
	XX=±.015 ANG.=±1°	DRN. MAH	ENG. APPR.	
UMENTS INC. D 44139	XXX=±.005 FRAC.=±1/64	MATERIAL		SIZE D NO. 2001-140-170
	SURFACE MAX. 63	FINISH		

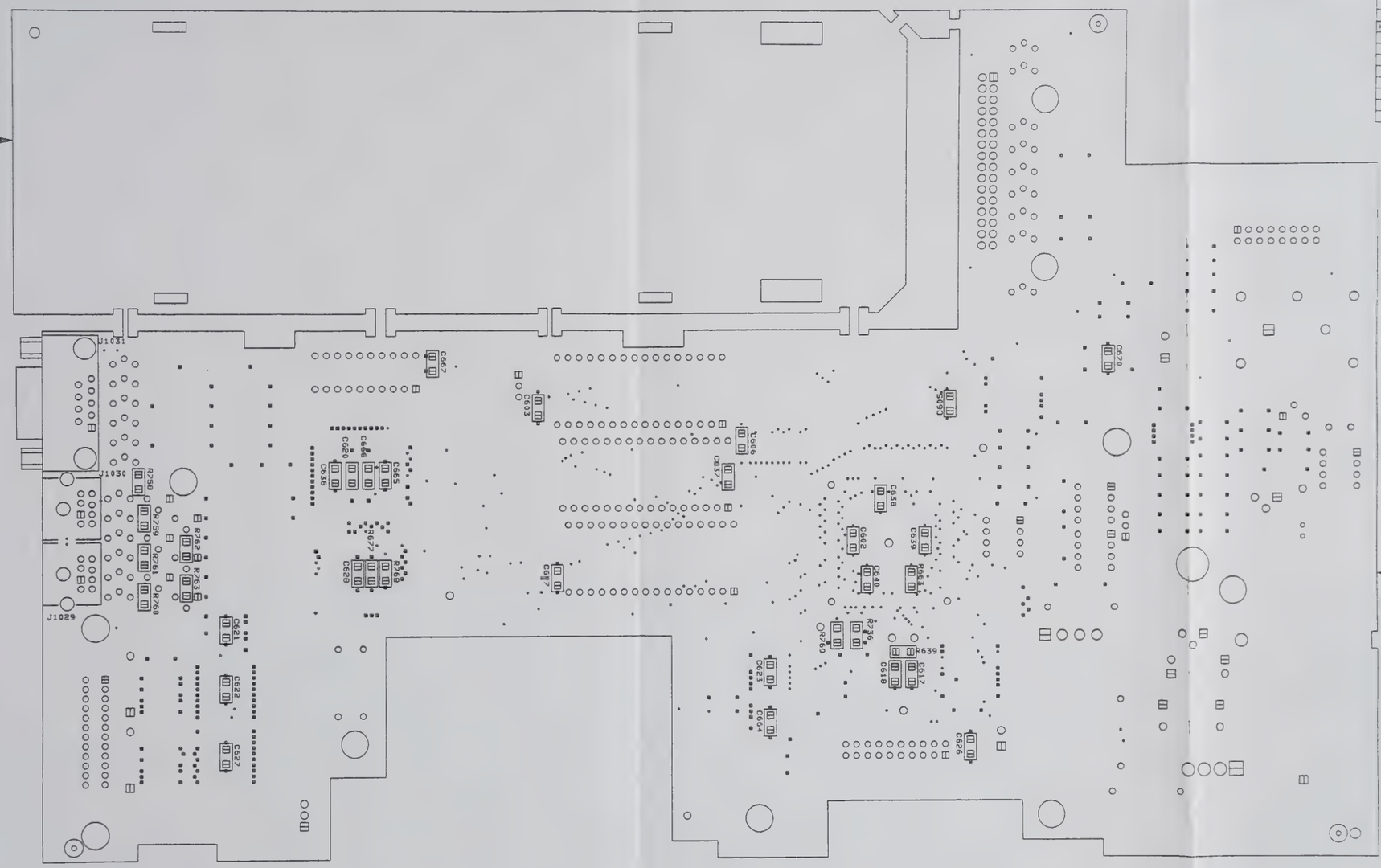
ORIGINAL IF RED H PG.2 OF 2

4-18b

NO. 2001-140-170

BOTTOM SIDE COMPONENTS

2001-171
(SCANNER BOARD)



2001-142
(DIGITAL BOARD)

2001-170 (SCANNER BOARD) REVISION CONTROL				
LTR.	ECO NO.	REVISION	ENG.	DATE
D	911015	RELEASED	MS	10/15/91
E	14912	REVISED	S2	11/20/91
E1	15012	RELOCATED MC-612 TO TOP SIDE	S2	1/2/92
F	15066	REVISED	S2	2/25/92
F1	17051	REVISED SEE PG.1		8-14-95

2001-140 (DIGITAL BOARD) REVISION CONTROL				
LTR.	ECO NO.	REVISION	ENG.	DATE
E	911015	RELEASED	MS	10/15/91
F	14917	REVISED	S2	11/20/91
F1	15012	SEE PAGE 1	S2	1/2/92
G	15042	REVISED	MS	1/11/92
H	15066	REVISED	S2	2/25/92
J	15329	CHG'D ARTWORK FROM REV H TO J.	AS	6/5/92
J1	15473	SEE PAGE 1	S2	10/2/92
J2	15524	SEE PAGE 1	S2	11/12/92
KDEV		ARTWORK WAS REV J.		
K	15583	ARTWORK WAS REV KDEV. ADDED C603	AS	1/12/93
K1	15736	SEE PAGE 1	AS	3/4/93
K2	16015	SEE PAGE 1	S2	8/2/93
K3	16057	SEE PAGE 1	S2	9/27/93
K4	16150	SEE PAGE 1	S2	10/28/93
K5	16409	SEE PAGE 1	S2	3/14/94
K6	16766	SEE PAGE 1	S2	10/11/94
K7	17540	SEE PAGE 1	S2	7/27/95

NOTE: FOR MORE COMPONENT INFORMATION REFER TO 2001 PRODUCT STRUCTURE.

2001	
MODEL	NEXT ASSEMBLY QTY.

USED ON

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 10/15/91	SCALE 2:1	TITLE	COMPONENT LAYOUT, DIGITAL BOARD & SCANNER BOARD
KEITHLEY KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1° / XXX=±.005 FRAC.=±1/64 / SURFACE MAX. 63	DRN. MAW	ENG. APPR.	SIZE D	NO. 2001-140-170
		MATERIAL			
		FINISH			

ORIGINAL IN RED H PG.2 OF 2

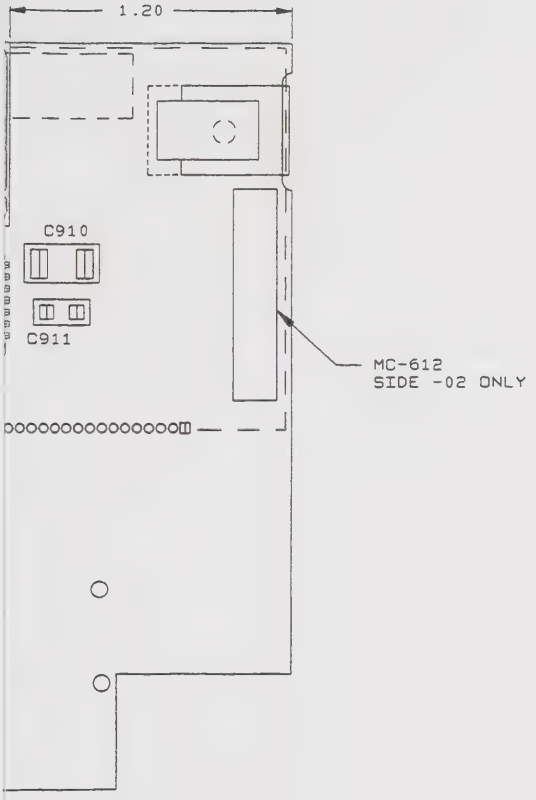
4-18b

Table 4-4
Model 2001 display board, parts list

Circuit Desig.	Description	Keithley Part No.
	CLIP, GROUND	2001-352B
	VACUUM FLUORESCENT DISPLAY	DD-51C
C901	CAP,22UF, 20%, 6.3,TANTALUM(C6032)	C-417-22
C902,904,907,908,910	CAP, .1UF, 20%,100V, CERAMIC (1812)	C-436-.1
C903,905,906,909,911	CAP,.1UF, 20%,50V,CERAMIC(1206)	C-418-.1
P1033	CABLE ASSEMBLY	CA-62-4A
R901	RES NET, 15K, 2%, 1.875W(SOMIC)	TF-219-15K
R902	RES, 13K, 5%,125MW, METAL FILM(1206)	R-375-13K
U901,904,905	IC, LATCHED DRIVERS,UCN-5812EPF-1(PLCC)	IC-732
U902	PROGRAM	7001-800-**
U903	IC, 32-BIT, SERIAL UCN5818EPF-1(PLCC)	IC-830

** Order present firmware revision level for main CPU (i.e., 2001-801-A05).

LTR.	ECO NO.	REVISION	ENG.	DATE
C	910730	RELEASED	MS	7/22/91
D	14842	REVISED	SZ	10/14/91
E	15043	REVISED	SZ	1/17/92
F	15182	CHG'D ARTWORK FROM REV E TO F.	AS	4/24/92
F1	15352	RELOCATED MC-612 & REVISED TP-12-1	AS	6/23/92
G	15406	CHG'D ARTWORK FROM REV F TO G.	AS	7/27/92
H	15483	CHG'D ARTWORK FROM REV G TO H. RELOCATED TOOLING HOLES. DELETED EXCESS MATERIAL.	AS	10/27/92
H1	16802	ADDED 7001-800A02.	SZ	11/1/94
H2	16924	ADDED (2) FE-27'S		7-2-95



2001		
MODEL	NEXT ASSEMBLY	QTY.
	USED ON	

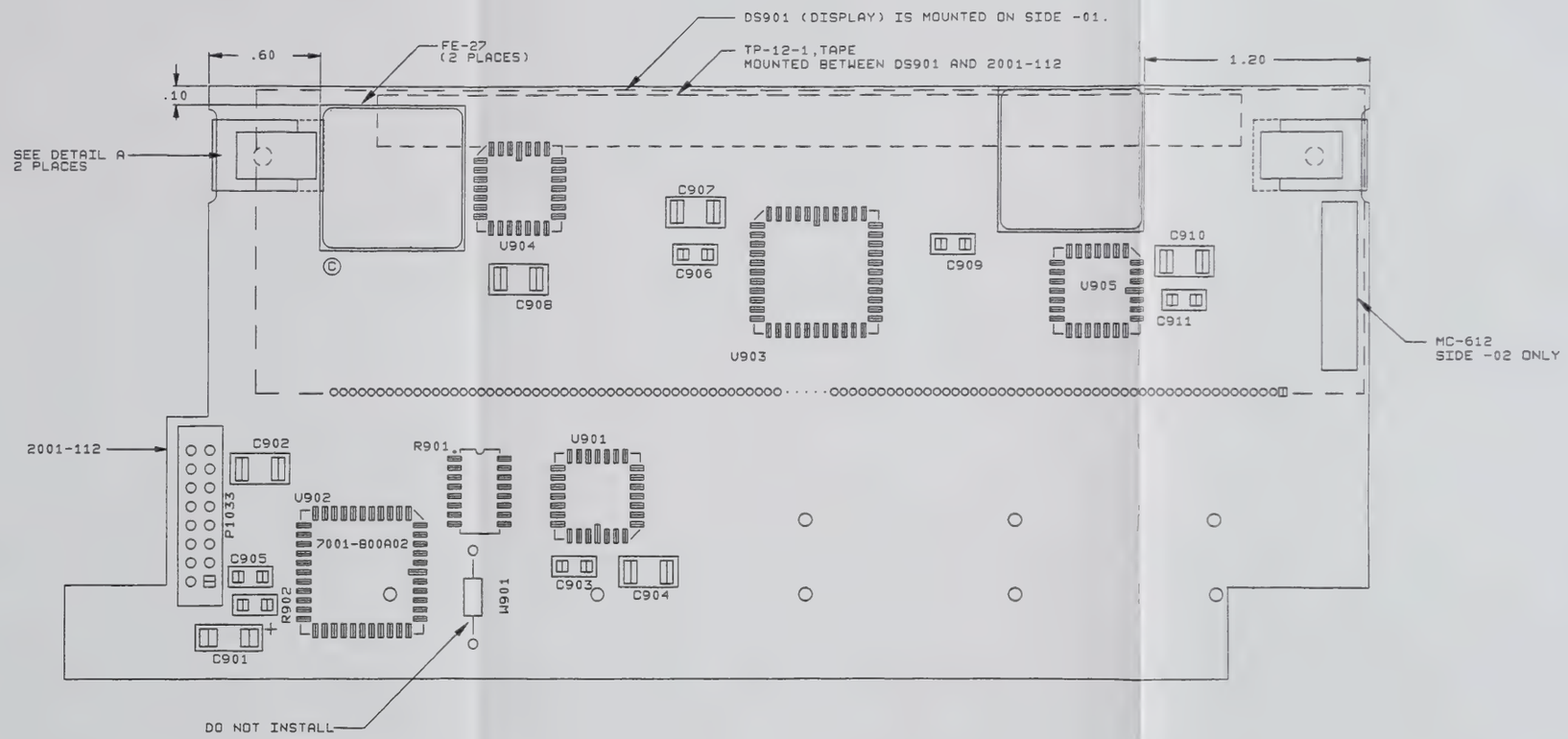
RANGES PECIFIED	DATE 6/25/91	SCALE 2:1	TITLE COMPONENT LAYOUT, DISPLAY BOARD
ANG. = ±1°	DRN. MAH	ENG. APPR.	
AC. = ±1/64	MATERIAL	C	NO. 2001-110
3/	FINISH		

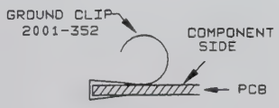
4-20

ORIGINAL IF PER

2001-110 ON

LTR.	ECO NO.	REVISION	ENG.	DATE
C	910730	RELEASED	MS	7/22/91
D	14842	REVISED	SZ	10/14/91
E	15043	REVISED	SZ	1/17/92
F	15182	CHG'D ARTWORK FROM REV E TO F.	AS	4/24/92
F1	15352	RELOCATED MC-612 & REVISED TP-12-1	AS	6/23/92
G	15406	CHG'D ARTWORK FROM REV F TO G.	AS	7/27/92
H	15483	CHG'D ARTWORK FROM REV G TO H. RELOCATED TOOLING HOLES. DELETED EXCESS MATERIAL.	AS	10/27/92
H1	16802	ADDED 7001-800A02.	SZ	11/1/94
H2	16924	ADDED (2) FE-27'S		3-2-95





DETAIL A

MODEL	NEXT ASSEMBLY	QTY.
2001		

USED ON

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 6/25/91	SCALE 2:1	TITLE COMPONENT LAYOUT, DISPLAY BOARD
KEITHLEY KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. MAH	ENG. APPR.	
	XXX=±.005 FRAC.=±1/64	MATERIAL		NO. C 2001-110
	SURFACE MAX. 63	FINISH		

4-20

ORIGINAL IS RED

Table 4-5
Model 2001 miscellaneous, parts list

Description	Keithley Part no.
BEZEL, REAR	428-303
BRACKET, REAR PANEL	2001-328
BUMBER	FE-27A
CARD GUIDE, LONG	2001-315
CARD GUIDE, SHORT	2001-316
CHOKE	CH-58-1
CLIP, REGULATOR	2001-343
CONDUCTIVE RUBBER SWITCH	2001-318
CONNECTOR	CS-236
CONNECTOR	CS-276
COVER	2001-360
DISPLAY LENS	2001-317
FILTER, FAN	2001-353
FOOT	428-319
FOOT, EXTRUDED	FE-22
FOOT, RUBBER	FE-6
FRONT PANEL ASSEMBLY	2001-061
FRONT PANEL	2001-302
FRONT/REAR SWITCH ROD	2001-322
FUSE, 2A,250V, FAST-BLO(5X20MM)	FU-48
GROMMET	GR-48-1
HANDLE	428-329
HANDLE TO CASE FASTENER	FA-230-2
HOLDER, FERRITE	2001-367
IEEE CONNECTOR, HARDWARE KIT	CS-713
INSULATOR, REGULATOR	2001-359
JACK, CURRENT INPUT	2001-312
LEXAN, ANALOG BOTTOM SHIELD (FOR 2001-339)	2001-340
LEXAN SHIELD, CHASSIS LEFT	2001-326
LEXAN SHIELD, CHASSIS-RIGHT	2001-336
LINE CORD	CO-7
LUG	LU-88
MOUNTING EAR, LEFT	428-338
MOUNTING EAR, RIGHT	428-328
OVERLAY, INPUTS	2001-310
PC BOARD STOP	2001-335
PLASTIC PLUG (FOR SCANNER COVER PLATE)	FA-240
POWER ROD	2001-320
PRINTED, FRONT PANEL	2001-356
SHIELDED, ANALOG BOTTOM SHIELD	2001-339
SHIELDED, ANALOG TOP SHIELD	2001-338
REAR BEZEL TO CHASSIS CAPTIVE PANEL SCREW	FA-232-1
RFI CLIP, CHASSIS	2001-366-14
RFI CLIP, CHASSIS	2001-366-5
TRANSFORMER	TR-280
TRANSFORMER BRACKET	2001-308

Table 4-5 (continued)
Model 2001 miscellaneous, parts list

Description	Keithley Part no.
"D" CONN. REAR OF DIGITAL BOARD SCREWLOCK, FEMALE	CS-725
#12 PVC- 4 1/8" FAN, DC BRUSHLESS, 12VDC, 100mA	FN-26
CONN, AC RECEPTACLE (LINE FILTER)	LF-6-1
BANANA JACK, PUSH-IN, RED	BJ-13-2
BANANA JACK, PUSH-IN, BLACK	BJ-13-0
BANANA JACK, PUSH-IN, WHITE	BJ-13-9
CONN, MOLEX HEADER	CS-716-3
CONNECTOR, HOUSING	CS-638-3

A

Model 2001 Specifications

Model 2001 Specifications

The following pages contain the complete specifications for the 2001. Every effort has been made to make these specifications complete by characterizing its performance under the variety of conditions often encountered in production, engineering and research.

The 2001 provides 5-minute, 1-hour, 24-hour, 90-day, 1-year, and 2-year specifications, with full specifications for the 90-day, 1-year and 2-year specifications. This allows the user to utilize 90-day, 1-year, or 2-year recommended calibration intervals, depending upon the level of accuracy desired. As a general rule, the 2001's 2-year performance exceeds a 5½-digit DMM's 90-day, 180-day or 1-year specifications. 6½- or 7½-digit performance is assured using 90-day or 1-year specifications.

ABSOLUTE ACCURACY

To minimize confusion, *all 90-day, 1-year and 2-year 2001 specifications are absolute accuracy,* traceable to NIST based on factory calibration. Higher accuracies are possible, based on your calibration sources. For example, calibrating with a 10V primary standard rather than a 20V calibrator will reduce calibration uncertainty, and can thereby improve total 2001 accuracy for measurements up to 50% of range. Refer to the 2001 calibration procedure for details.

TYPICAL ACCURACIES

Accuracy can be specified as typical or warranted. All specifications shown are warranted unless specifically noted.

Almost 99% of the 2001's specifications are warranted specifications. In some cases it is not possible to obtain sources to maintain traceability on the performance of every unit in production on some measurements (e.g., high-voltage, high-frequency signal sources with sufficient accuracy do not exist). Since these values cannot be verified in production, the values are listed as typical.

2001 SPECIFIED CALIBRATION INTERVALS

MEASUREMENT FUNCTION	24 HOUR[1]	90 DAY[2]	1 YEAR[2]	2 YEAR[2]
DC Volts	•	•	•	•
DC Volts Peak Spikes		•[3]	•	•
AC Volts rms		•[3]	•	•
AC Volts Peak		•[3]	•	•
AC Volts Average		•[3]	•	•
AC Volts Crest Factor		•[3]	•	•
Ohms	•	•	•	•
DC Current	•	•	•	•
DC In-Circuit Current		•	•	•
AC Current		•[3]	•	•
Frequency		•	•	•
Temperature (Thermocouple)		•	•	•
Temperature (RTD)		•	•	•

[1] For T_{CAL} ±1°C.
[2] For T_{CAL} ±5°C.
[3] For ±2°C of last AC self cal.

DCV INPUT CHARACTERISTICS AND ACCURACY

RANGE	FULL SCALE	RESOLUTION	DEFAULT RESOLUTION	INPUT RESISTANCE	ACCURACY[1] ± (ppm of reading + ppm of range) 5 Minutes[12]	24 Hours[2]	90 Days[3]	1 Year[3]	2 Years[3]	TEMPERATURE COEFFICIENT ± (ppm of reading + ppm of range)/°C Outside T_{CAL} ± 5°C
200 mV[4]	±210.00000	10 nV	100 nV	>10 GΩ	3 + 3	10 + 6	25 + 6	37 + 6	50 + 6	3.3 +1.5
2 V	±2.1000000	100 nV	1 µV	>10 GΩ	2 + 1.5	7 + 2	18 + 2	25 + 2	32 + 2	2.6 +0.15
20 V	±21.000000	1 µV	10 µV	>10 GΩ	2 + 1.5	7 + 4	18 + 4	24 + 4	32 + 4	2.6 +0.7
200 V	±210.00000	10 µV	100 µV	10 MΩ ±1%	2 + 1.5	13 + 3	27 + 3	38 + 3	52 + 3	4.3 +1
1000 V	±1100.0000	100 µV	1 mV	10 MΩ ±1%	10 + 1.5	17 + 6	31 + 6	41 + 6	55 + 6	4.1 +1

DC VOLTAGE UNCERTAINTY = ±[(ppm of reading) × (measured value) + (ppm of range) × (range used)] / 1,000,000.

% ACCURACY = (ppm accuracy) /10,000.

1PPM OF RANGE = 2 counts for ranges up to 200V, 1 count on 1000V range at 6½ digits.

SPEED AND ACCURACY[5] 90 Days

RANGE	ACCURACY ± (ppm of reading + ppm of range + ppm of range rms noise[10]) 1PLC DFILT On, 10 Readings	1PLC DFILT Off	0.1PLC DFILT Off	0.01PLC[11] DFILT Off
200 mV[4]	25+6+0	25+6+0.6	25+30+10	100+200+15
2 V	18+2+0	18+2+0.2	18+25+1	130+200+3
20 V	18+4+0	18+4+0.3	18+20+0.5	130+200+3
200 V	27+3+0	27+5+0.3	27+20+0.8	130+200+3
1000 V	31+6+0	31+6+0.1	31+21+0.5	90+200+2

PLC = power line cycle; DFILT = digital filter

NOISE REJECTION (dB)

SPEED (Number of Power Line Cycles)	AC and DC CMRR[6] Line Sync On[7]	Internal Trigger[8]	AC NMRR Line Sync On[7] 25-Reading DFILT On	Line Sync On[7] DFILT Off	Internal Trigger[8] DFILT Off
NPLC = 10	140	120	90	80	60
NPLC ≥ 1	140	120	90	80	60
NPLC < 1	60	50	30	20	0

Effective noise is reduced by a factor of 10 for every 20dB of noise rejection (140dB reduces effective noise by 10,000,000:1).

CMRR is rejection of undesirable AC or DC signal between LO and earth. NMRR is rejection of undesirable AC signal between HI and LO.

DCV READING RATES[9,10]

200mV, 2V, 200V Ranges

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS/SECOND TO MEMORY Auto Zero Off	Auto Zero On	READINGS/SECOND TO IEEE-488 Auto Zero Off	Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	Auto Zero On
10	167 ms (200 ms)	28	7½	6 (5.1)	2 (1.7)	6	2 (1.6)	6 (4.1)	2 (1.6)
2	33.4 ms (40 ms)	26	7½	30 (25)	9 (7.6)	28 (23)	9 (7.3)	27 (22)	8 (7.2)
1	16.7 ms (20 ms)	25	6½	58 (48)	44 (34)	54 (45)	41 (32)	49 (41)	37 (30)
0.2	3.34 ms (4 ms)	22	6½	214 (186)	127 (112)	183 (162)	104 (101)	140 (126)	88 (85)
0.1	1.67 ms (2 ms)	21	5½	272 (272)	150 (148)	228 (225)	129 (123)	156 (153)	100 (96)
0.02	334 µs (400 µs)	19	5½	284 (287)	156 (155)	230 (230)	136 (134)	158 (156)	104 (103)
0.01	167 µs (167 µs)	16	4½	417 (417)	157 (157)	317 (317)	137 (134)	198 (198)	105 (103)
0.01[11]	167 µs (167 µs)	16	4½	2000 (2000)		2000 (2000)			

20V, 1000V Ranges

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS/SECOND TO MEMORY Auto Zero Off	Auto Zero On	READINGS/SECOND TO IEEE-488 Auto Zero Off	Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	Auto Zero On
10	167 ms (200 ms)	28	7½	6 (5.1)	2 (1.7)	6	2 (1.6)	6	2 (1.6)
2	33.4 ms (40 ms)	26	7½	30 (25)	9 (8.2)	28 (23)	9 (7.8)	27 (22)	9 (7.7)
1	16.7 ms (20 ms)	25	6½	57 (48)	42 (38)	54 (45)	43 (35)	48 (41)	39 (32)
0.2	3.34 ms (4 ms)	22	6½	201 (186)	102 (113)	173 (162)	102 (99)	129 (127)	84 (83)
0.1	1.67 ms (2 ms)	21	5½	201 (201)	126 (116)	175 (173)	105 (105)	129 (128)	86 (86)
0.02	334 µs (400 µs)	19	5½	227 (227)	129 (129)	178 (178)	114 (114)	138 (138)	90 (90)
0.01	167 µs (167 µs)	16	4½	422 (422)	130 (130)	333 (333)	117 (117)	199 (199)	95 (95)
0.01[11]	167 µs (167 µs)	16	4½	2000 (2000)		2000 (2000)			

SETTLING CHARACTERISTICS: <500µs to 10ppm of step size. Reading settling times are affected by source impedance and cable dielectric absorption characteristics. Add 10ppm of range for first reading after range change.

ZERO STABILITY: Typical variation in zero reading, 1 hour, T_{REF} ±1°C, 6½-digit default resolution, 10-reading digital filter:

Range	ZERO STABILITY 1 Power Line Cycle Integration	10 Power Line Cycle Integration
2V – 1000V	±3 counts	±2 counts
200 mV	±5 counts	±3 counts

ISOLATED POLARITY REVERSAL ERROR: This is the portion of the instrument error that is seen when high and low are reversed when driven by an isolated source. This is not an additional error—it is included in the overall instrument accuracy spec. **Reversal Error:** <2 counts at 10V input at 6½ digits, 10 power line cycles, 10-reading digital filter.

INPUT BIAS CURRENT: <100pA at 25°C.

LINEARITY: <1ppm of range typical, <2ppm maximum.

AUTORANGING: Autoranges up at 105% of range, down at 10% of range.

DC VOLTS NOTES

1. Specifications are for 1 power line cycle, Auto Zero on, 10-reading digital filter, except as noted.
2. For T_{CAL} ±1°C, following 55-minute warm-up. T_{CAL} is ambient temperature at calibration, which is 23°C from factory.
3. For T_{CAL} ±5°C, following 55-minute warm-up. Specifications include factory traceability to US NIST.
4. When properly zeroed using REL function.
5. For T_{CAL} ±5°C, 90-day accuracy. 1-year or 2-year accuracy can be found by applying the same speed accuracy ppm changes to the 1-year or 2-year base accuracy.
6. Applies for 1kΩ imbalance in the LO lead. For 400Hz operation, subtract 10dB.
7. For noise synchronous to the line frequency.
8. For line frequency ±0.1%.
9. See Operating Speed section for additional detail. For DELAY=0, internal trigger, digital filter off, display off (or display in "hold" mode). Aperture is reciprocal of line frequency. These rates are for 60Hz and (50Hz).
10. Typical values.
11. In burst mode, display off. Burst mode requires Auto Zero refresh (by changing resolution or measurement function) once every 24 hours.
12. DCV Transfer Stability typical applications are standard cell comparisons and relative accuracy measurements. Specs apply for 10 power line cycles, 20-reading digital filter, autozero on with type synchronous, fixed range following 2-hour warm-up at full scale to 10% of full scale, at T_{REF} ± 1°C (T_{REF} is the initial ambient temperature). Specifications on the 1000V range are for measurements within 5% of the initial measurement value and following measurement settling.

DCV PEAK SPIKES MEASUREMENT

REPETITIVE SPIKES ACCURACY[1] 90 Days, ±2°C from last AC self-cal ±(% of reading+% of range)

RANGE	0–1kHz[4]	1kHz–10kHz	10kHz–30kHz	30kHz–50kHz	50kHz–100kHz	100kHz–300kHz	300kHz–500kHz	500kHz–750kHz	750kHz–1MHz	TEMPERATURE COEFFICIENT ±(% of reading+% of range)/°C Outside T_{CAL} ±2°C
200 mV	0.08+0.7	0.08+0.7	0.1 +0.7	0.15+0.7	0.25+0.7	1.0+0.7	2.5+0.7	5.5+0.7	9+0.7	0.002+0.03
2 V	0.08+0.3	0.08+0.3	0.1 +0.3	0.15+0.3	0.25+0.3	1.0+0.3	2.5+0.3	5.5+0.3	9+0.3	0.002+0.03
20 V	0.09+0.7	0.1 +0.7	0.12+0.7	0.17+0.7	0.25+0.7	1.0+0.7	2.5+0.7	5.5+0.7	9+0.7	0.004+0.03
200 V[3]	0.09+0.3	0.1 +0.3	0.12+0.3	0.17+0.3	0.25+0.3	1.0+0.3[2]	2.5+0.3[2]	5.5+0.3[2]	9+0.3[2]	0.004+0.03
1000 V[3]	0.1 +0.6	0.13+0.6	0.16+0.6	0.25+0.6[2]	0.5 +0.6[2]					0.01 +0.02
Max. % of Range	±125%	±125%	±125%	±125%	±125%	±125%	±125%	±100%	±75%	

REPETITIVE SPIKES ACCURACY[1] 1 or 2 Years, T_{CAL} ±5°C ±(% of reading+% of range)

RANGE	0–1kHz[4]	1kHz–10kHz	10kHz–30kHz	30kHz–50kHz	50kHz–100kHz	100kHz–300kHz	300kHz–500kHz	500kHz–750kHz	750kHz–1MHz	TEMPERATURE COEFFICIENT ±(% of reading+% of range)/°C Outside T_{CAL} ±5°C
200 mV	0.08+0.7	0.09+0.7	0.1 +0.7	0.15+0.7	0.25+0.7	1.0+0.7	2.5+0.7	5.5+0.7	9+0.7	0.002+0.03
2 V	0.08+0.3	0.09+0.3	0.1 +0.3	0.15+0.3	0.25+0.3	1.0+0.3	2.5+0.3	5.5+0.3	9+0.3	0.002+0.03
20 V	0.1 +0.7	0.11+0.7	0.14+0.7	0.19+0.7	0.25+0.7	1.0+0.7	2.5+0.7	5.5+0.7	9+0.7	0.004+0.03
200 V[3]	0.1 +0.3	0.11+0.3	0.14+0.3	0.19+0.3	0.25+0.3	1.0+0.3[2]	2.5+0.3[2]	5.5+0.3[2]	9+0.3[2]	0.004+0.03
1000 V[3]	0.12+0.6	0.16+0.6	0.2 +0.6	0.25+0.6[2]	0.5 +0.6[2]					0.01 +0.02
Max. % of Range	±125%	±125%	±125%	±125%	±125%	±125%	±125%	±100%	±75%	

DEFAULT MEASUREMENT RESOLUTION: 3½ digits.

MAXIMUM INPUT: ±1100V peak value, 2×10^7V•Hz (for inputs above 20V).

NON-REPETITIVE SPIKES: 10% of range per µs typical slew rate.

SPIKE WIDTH: Specifications apply for spikes ≥1µs.

RANGE CONTROL: In Multiple Display mode, voltage range is the same as DCV range.

SPIKES MEASUREMENT WINDOW: Default is 100ms per reading (settable from 0.1 to 9.9s in Primary Display mode).

INPUT CHARACTERISTICS: Same as ACV input characteristics.

SPIKES DISPLAY: Access as multiple display on DC Volts. First option presents positive peak spikes and highest spike since reset. Second option presents negative spikes and lowest spike. Highest and lowest spike can be reset by pressing DCV function button. Third option displays the maximum and minimum levels of the input signal. Spikes displays are also available through CONFIG-ACV-ACTYPE as primary displays.

DCV PEAK SPIKES NOTES

1. Specifications apply for 10-reading digital filter. If no filter is used, add 0.25% of range typical uncertainty.
2. Typical values.
3. Add 0.001% of reading × (V_{IN}/100V)² additional uncertainty for inputs above 100V.
4. Specifications assume AC+DC coupling for frequencies below 200Hz. Below 20Hz add 0.1% of reading additional uncertainty.

AC VOLTS

AC magnitude: RMS or Average. Peak and Crest Factor measurements also available.

ACV INPUT CHARACTERISTICS

RMS RANGE	PEAK INPUT	FULL SCALE RMS	RESOLUTION	DEFAULT RESOLUTION	INPUT IMPEDANCE	TEMPERATURE COEFFICIENT[2] ±(% of reading + % of range) / °C Outside T_{CAL} ±5°C
200 mV	1 V	210.0000	100 nV	1 µV	1MΩ ±2% with <140pF	0.004 + 0.001
2 V	8V	2.100000	1 µV	10 µV	1MΩ ±2% with <140pF	0.004 + 0.001
20 V	100 V	21.00000	10 µV	100 µV	1MΩ ±2% with <140pF	0.006 + 0.001
200 V	800 V	210.0000	100 µV	1 mV	1MΩ ±2% with <140pF	0.006 + 0.001
750 V	1100 V	775.000	1 mV	10 mV	1MΩ ±2% with <140pF	0.012 + 0.001

AC VOLTAGE UNCERTAINTY = ±[(% of reading) × (measured value) + (% of range) × (range used)] / 100.

PPM ACCURACY = (% accuracy) × 10,000.

0.015% OF RANGE = 30 counts for ranges up to 200V and 113 counts on 750V range at 5½ digits.

LOW FREQUENCY MODE RMS[1] 90 Days, ±2°C from last AC self-cal, for 1% to 100% of range[3] ±(% of reading + % of range)

RANGE	1–10Hz[5]	10–50Hz	50–100Hz	0.1–2kHz	2–10kHz	10–30kHz	30–50kHz	50–100kHz	100–200kHz	0.2–1MHz	1–2MHz
200 mV	0.09+0.015	0.04+0.015	0.03+0.015	0.03+0.015	0.03+0.015	0.035+0.015	0.05+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
2 V	0.09+0.015	0.04+0.015	0.03+0.015	0.03+0.015	0.03+0.015	0.035+0.015	0.05+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
20 V	0.1 +0.015	0.05+0.015	0.04+0.015	0.04+0.015	0.06+0.015	0.08 +0.015	0.1 +0.015	0.3+0.015	0.75+0.025	4+0.2	7+0.2[5]
200 V[4]	0.1 +0.015	0.05+0.015	0.04+0.015	0.04+0.015	0.06+0.015	0.08 +0.015	0.1 +0.015	0.3+0.015	0.75+0.025[5]	4+0.2[5]	
750 V[4]	0.13+0.015	0.09+0.015	0.08+0.015	0.08+0.015	0.09+0.015	0.12 +0.015	0.15+0.015[5]	0.5+0.015[5]			

LOW FREQUENCY MODE RMS[1] 1 or 2 Years, T_{CAL} ±5°C for 1% to 100% of range[3] ±(% of reading + % of range)

RANGE	1–10Hz[5]	10–50Hz	50–100Hz	0.1–2kHz	2–10kHz	10–30kHz	30–50kHz	50–100kHz	100–200kHz	0.2–1MHz	1–2MHz
200 mV	0.11+0.015	0.06+0.015	0.05+0.015	0.05+0.015	0.05 +0.015	0.05+0.015	0.06+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
2 V	0.11+0.015	0.06+0.015	0.05+0.015	0.05+0.015	0.05 +0.015	0.05+0.015	0.06+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
20 V	0.12+0.015	0.07+0.015	0.06+0.015	0.06+0.015	0.085+0.015	0.12+0.015	0.13+0.015	0.3+0.015	0.75+0.025	4+0.2	7+0.2[5]
200 V[4]	0.12+0.015	0.07+0.015	0.06+0.015	0.06+0.015	0.085+0.015	0.12+0.015	0.13+0.015	0.3+0.015	0.75+0.025[5]	4+0.2[5]	
750 V[4]	0.15+0.015	0.11+0.015	0.1 +0.015	0.1 +0.015	0.13 +0.015	0.18+0.015	0.22+0.015[5]	0.5+0.015[5]			

AC VOLTS (cont'd)

NORMAL MODE RMS[1] 90 Days, ±2°C from last AC self-cal for 1% to 100% of range[3] ±(% of reading + % of range)

RANGE	20–50Hz	50–100Hz	0.1–2kHz	2–10kHz	10–30kHz	30–50kHz	50–100kHz	100–200kHz	0.2–1MHz	1–2MHz
200 mV	0.25+0.015	0.07+0.015	0.03+0.015	0.03+0.015	0.035+0.015	0.05+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
2 V	0.25+0.015	0.07+0.015	0.03+0.015	0.03+0.015	0.035+0.015	0.05+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
20 V	0.25+0.015	0.07+0.015	0.04+0.015	0.06+0.015	0.08 +0.015	0.1 +0.015	0.3+0.015	0.75+0.025	4+0.2	7+0.2[5]
200 V[4]	0.25+0.015	0.07+0.015	0.04+0.015	0.06+0.015	0.08 +0.015	0.1 +0.015	0.3+0.015	0.75+0.025[5]	4+0.2[5]	
750 V[4]	0.25+0.015	0.1 +0.015	0.08+0.015	0.09+0.015	0.12 +0.015	0.15+0.015[5]	0.5+0.015[5]			

NORMAL MODE RMS[1] 1 or 2 Years, T_{CAL} ±5°C for 1% to 100% of range[3] ±(% of reading + % of range)

RANGE	20–50Hz	50–100Hz	0.1–2kHz	2–10kHz	10–30kHz	30–50kHz	50–100kHz	100–200kHz	0.2–1MHz	1–2MHz
200 mV	0.25+0.015	0.08+0.015	0.05+0.015	0.05 +0.015	0.05+0.015	0.06+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
2 V	0.25+0.015	0.08+0.015	0.05+0.015	0.05 +0.015	0.05+0.015	0.06+0.015	0.3+0.015	0.75+0.025	2+0.1	5+0.2
20 V	0.25+0.015	0.08+0.015	0.06+0.015	0.085+0.015	0.12+0.015	0.13+0.015	0.3+0.015	0.75+0.025	4+0.2	7+0.2[5]
200 V[4]	0.25+0.015	0.08+0.015	0.06+0.015	0.085+0.015	0.12+0.015	0.13+0.015	0.3+0.015	0.75+0.025[5]	4+0.2[5]	
750 V[4]	0.27+0.015	0.11+0.015	0.1 +0.015	0.13 +0.015	0.18+0.015	0.22+0.015[5]	0.5+0.015[5]			

dB ACCURACY RMS ±dB, 90 Days, 1 or 2 Years, T_{CAL} ±5°C, Reference=1V, Autoranging, Low Frequency Mode, AC+DC Coupling

INPUT	1–100Hz	0.1–30kHz	30–100kHz	100–200kHz	0.2–1MHz	1–2MHz
–54 to–40 dB (2mV to 10mV)	0.230	0.225	0.236	0.355		
–40 to–34 dB (10mV to 20mV)	0.036	0.031	0.041	0.088		
–34 to 6 dB (20mV to 2 V)	0.023	0.018	0.028	0.066	0.265	0.630
6 to 26 dB (2 V to 20 V)	0.024	0.024	0.028	0.066	0.538	0.820[5]
26 to 46 dB (20 V to 200 V)	0.024	0.024	0.028	0.066[5]	0.538[5]	
46 to 57.8 dB (200 V to 775 V)	0.018	0.021	0.049[5]			

ACV READING RATES[5,6]

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS/SECOND TO MEMORY Auto Zero Off	READINGS/SECOND TO MEMORY Auto Zero On	READINGS/SECOND TO IEEE-488 Auto Zero Off	READINGS/SECOND TO IEEE-488 Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero On
10	167 ms (200 ms)	28	6½	6 (5.1)	2 (1.7)	2	2 (1.6)	2	2 (1.5)
2	33.4 ms (40 ms)	26	5½	30 (24)	9 (7.9)	28 (23)	9 (7.6)	27 (22)	9 (7.5)
1	16.7 ms (20 ms)	25	5½	57 (48)	38 (35)	53 (45)	36 (33)	48 (41)	34 (30)
0.1	1.67 ms (2 ms)	21	5½	136 (136)	70 (70)	122 (122)	64 (64)	98 (98)	56 (56)
0.01	167 µs (167 µs)	16	4½	140 (140)	71 (71)	127 (127)	66 (66)	99 (99)	58 (58)
0.01[8]	167 µs (167 µs)	16	4½	2000 (2000)		2000 (2000)			

AC COUPLING: For AC only coupling, add the following % of reading:

	1–10Hz	10–20Hz	20–50Hz	50–100Hz	100–200Hz
Normal Mode (rms, average)	—	—	0.41	0.07	0.015
Low Frequency Mode (rms)	0.1	0.01	0	0	0

For low frequency mode below 200Hz, specifications apply for sine wave inputs only.

AC+DC COUPLING: For DC>20% of AC rms voltage, apply the following additional uncertainty, multiplied by the ratio (DC/AC rms). Applies to rms and average measurements.

RANGE	% of Reading	% of Range
200mV, 20V	0.05	0.1
2V, 200V, 750V	0.07	0.01

AVERAGE ACV MEASUREMENT

Normal mode rms specifications apply from 10% to 100% of range, for 20Hz–1MHz. Add 0.025% of range for 50kHz–100kHz, 0.05% of range for 100kHz–200kHz, and 0.5% of range for 200kHz–1MHz.

ACV CREST FACTOR MEASUREMENT[11]

CREST FACTOR = Peak AC / rms AC.

CREST FACTOR RESOLUTION: 3 digits.

CREST FACTOR ACCURACY: Peak AC uncertainty + AC normal mode rms uncertainty.

MEASUREMENT TIME: 100ms plus rms measurement time.

INPUT CHARACTERISTICS: Same as ACV input.

CREST FACTOR FREQUENCY RANGE: 20Hz – 1MHz.

CREST FACTOR DISPLAY: Access as multiple display on AC volts.

HIGH CREST FACTOR ADDITIONAL ERROR ±(% of reading)

Applies to rms measurements.

CREST FACTOR:	1 – 2	2 – 3	3 – 4	4 – 5
ADDITIONAL ERROR:	0	0.1	0.2	0.4

ACV PEAK VALUE MEASUREMENT[10] REPETITIVE PEAK ACCURACY, ±(% of reading+% of range), 90 Days, 1 Year or 2 Years, T_{CAL} ±5°C

RANGE	20Hz–1kHz[9]	1kHz–10kHz	10kHz–30kHz	30kHz–50kHz	50kHz–100kHz	100kHz–300kHz	300kHz–500kHz	500kHz–750kHz	750kHz–1MHz	TEMPERATURE COEFFICIENT ±(% of reading+% of range)/°C Outside T_{CAL} ±5°C
200 mV	0.08+0.7	0.09+0.7	0.1 +0.7	0.15+0.7	0.25+0.7	1.0+0.7	2.5+0.7	5.5+0.7	9+0.7	0.002 + 0.03
2 V	0.08+0.3	0.09+0.3	0.1 +0.3	0.15+0.3	0.25+0.3	1.0+0.3	2.5+0.3	5.5+0.3	9+0.3	0.002 + 0.03
20 V	0.1 +0.7	0.11+0.7	0.14+0.7	0.19+0.7	0.25+0.7	1.0+0.7	2.5+0.7	5.5+0.7	9+0.7	0.004 + 0.03
200 V[4]	0.1 +0.3	0.11+0.3	0.14+0.3	0.19+0.3	0.25+0.3	1.0+0.3[5]	2.5+0.3[5]	5.5+0.3[5]	9+0.3[5]	0.004 + 0.03
750 V[4]	0.12+0.6	0.16+0.6	0.2 +0.6	0.25+0.6[5]	0.5 +0.6[5]					0.01 + 0.02
Valid % of Range[7]	10–400%	10–400%	10–400%	10–350%	10–350%	10–250%	10–150%	10–100%	7.5–75%	

DEFAULT MEASUREMENT RESOLUTION: 4 digits.

NON-REPETITIVE PEAK: 10% of range per µs typical slew rate for single spikes.

PEAK WIDTH: Specifications apply for all peaks ≥1µs.

PEAK MEASUREMENT WINDOW: 100ms per reading.

MAXIMUM INPUT: ±1100V peak, 2×10^7V•Hz (for inputs above 20V).

AC VOLTS (cont'd)

SETTLING CHARACTERISTICS:

Normal Mode (rms, avg.)	<300ms to 1% of step change <450ms to 0.1% of step change <500ms to 0.01% of step change
Low Frequency Mode (rms)	<5s to 0.1% of final value

COMMON MODE REJECTION: For 1kΩ imbalance in either lead: >60dB for line frequency ±0.1%.

MAXIMUM VOLT•Hz PRODUCT: 2×10^7V•Hz (for inputs above 20V).

AUTORANGING: Autoranges up at 105% of range, down at 10% of range.

AC VOLTS NOTES

1. Specifications apply for sinewave input, AC + DC coupling, 1 power line cycle, digital filter off, following 55 minute warm-up.
2. Temperature coefficient applies to rms or average readings. For frequencies above 100kHz, add 0.01% of reading/°C to temperature coefficient.
3. For 1% to 5% of range below 750V range, and for 1% to 7% of 750V range, add 0.01% to range uncertainty. For inputs from 200kHz to 2MHz, specifications apply above 10% of range.
4. Add 0.001% of reading × $(V_{IN}/100V)^2$ additional uncertainty above 100V rms.
5. Typical values.
6. For DELAY=0, digital filter off, display off (or display in "hold" mode). Internal Trigger, Normal mode. See Operating Speed section for additional detail. Aperture is reciprocal of line frequency. These rates are for 60Hz and (50Hz). Applies for rms and average mode. Low frequency mode rate is typically 0.2 readings per second.
7. For overrange readings 200–300% of range, add 0.1% of reading. For 300–400% of range, add 0.2% of reading.
8. In burst mode, display off. Burst mode requires Auto Zero refresh (by changing resolution or measurement function) once every 24 hours.
9. AC peak specifications assume AC + DC coupling for frequencies below 200Hz.
10. Specifications apply for 10 reading digital filter. If no filter is used, add 0.25% of range typical uncertainty.
11. Subject to peak input voltage specification.

OHMS

TWO-WIRE AND FOUR-WIRE OHMS (2W and 4W Ohms Functions)[13]

RANGE	FULL SCALE	RESOLUTION	DEFAULT RESOLUTION	CURRENT[1] SOURCE	OPEN CIRCUIT[12]	MAXIMUM LEAD RESISTANCE[2]	MAXIMUM OFFSET COMPENSATION[3]	TEMPERATURE COEFFICIENT ± (ppm of reading + ppm of range)/°C Outside T_{CAL} ± 5°
20 Ω	21.000000	1 μΩ	10 μΩ	9.2 mA	5 V	1.7 Ω	±0.2 V	8 + 1.5
200 Ω	210.00000	10 μΩ	100 μΩ	0.98 mA	5 V	12 Ω	±0.2 V	4 + 1.5
2 kΩ	2100.0000	100 μΩ	1 mΩ	0.98 mA	5 V	100 Ω	–0.2 V to +2 V	3.0 + 0.2
20 kΩ	21.000000	1 mΩ	10 mΩ	89 μA	5 V	1.5 kΩ	–0.2 V to +2 V	4 + 0.2
200 kΩ	210.00000	10 mΩ	100 mΩ	7 μA	5 V	1.5 kΩ		11 + 0.2
2 MΩ[4]	2.1000000	100 mΩ	1 Ω	770 nA	5 V	1.5 kΩ		25 + 0.2
20 MΩ[4]	21.000000	1 Ω	10 Ω	70 nA	5 V	1.5 kΩ		250 + 0.2
200 MΩ[4]	210.00000	10 Ω	100 Ω	4.4 nA	5 V	1.5 kΩ		4000 + 10
1 GΩ[4]	1.0500000	100 Ω	1 kΩ	4.4 nA	5 V	1.5 kΩ		4000 + 10

RESISTANCE ACCURACY[5] ± (ppm of reading + ppm of range)

RANGE	24 Hours[6]	90 Days[7]	1 Year[7]	2 Years[7]
20 Ω	29 + 7	52 + 7	72 + 7	110 + 7
200 Ω	24 + 7	36 + 7	56 + 7	90 + 7
2 kΩ	22 + 4	33 + 4	50 + 4	80 + 4.5
20 kΩ	19 + 4	32 + 4	50 + 4	80 + 4.5
200 kΩ	20 + 4.5	72 + 4.5	90 + 4.5	130 + 5
2 MΩ[4]	50 + 4.5	110 + 4.5	160 + 4.5	230 + 5
20 MΩ[4]	160 + 4.5	560 + 4.5	900 + 4.5	1100 + 5
200 MΩ[4]	3000 + 100	10000 + 100	20000 + 100	30000 + 100
1 GΩ[4]	9000 + 100	20000 + 100	40000 + 100	60000 + 100

RESISTANCE UNCERTAINTY = ± [(ppm of reading) × (measured value) + (ppm of range) × (range used)] / 1,000,000.

% ACCURACY = (ppm accuracy) / 10,000.

1PPM OF RANGE = 2 counts for ranges up to 200MΩ and 1 count on 1GΩ range at 6½ digits.

SPEED AND ACCURACY[9] 90 Days

RANGE	ACCURACY ± (ppm of reading + ppm of range + ppm of range rms noise[12]) 1PLC DFILT Off	0.1PLC[11] DFILT Off	0.01PLC[8,11] DFILT Off
20 Ω	52+ 7+0.6	52+ 30+10	110+200+ 35
200 Ω	36+ 7+0.6	36+ 30+10	110+200+ 35
2 kΩ	33+ 4+0.2	33+ 24+ 1	130+230+ 5
20 kΩ	32+ 4+0.2	32+ 24+ 2	130+230+ 5
200 kΩ	72+ 4.5+0.5	72+ 25+ 4	150+300+ 10
2 MΩ[4]	110+ 4.5+ 2	110+ 25+15	150+300+150
20 MΩ[4]	560+ 4.5+ 5	560+ 30+20	560+300+150
200 MΩ[4]	10,000+100+ 40	10,000+120+80	10,000+700+250
1 GΩ[4]	20,000+100+ 40	20,000+120+80	20,000+700+250

PLC = Power Line Cycles. DFILT = Digital Filter.

2-WIRE ACCURACY[7] ± (ppm of range)

RANGE	20 Ω	200 Ω	2 kΩ
ADDITIONAL UNCERTAINTY (Inside T_{CAL} ± 5°C)	300 ppm	30 ppm	3 ppm
TEMPERATURE COEFFICIENT (outside T_{CAL} ± 5°C)	70ppm/°C	7ppm/°C	0.7ppm/°C

SETTLING CHARACTERISTICS: For first reading following step change, add the total 90-day measurement error for the present range. Pre-programmed settling delay times are for <200pF external circuit capacitance. For 200MΩ and 1GΩ ranges, add total 1 year errors for first reading following step change. Reading settling times are affected by source impedance and cable dielectric absorption characteristics.

OHMS MEASUREMENT METHOD: Constant current.

OFFSET COMPENSATION: Available on 20Ω – 20kΩ ranges.

OHMS VOLTAGE DROP MEASUREMENT: Available as a multiple display.

AUTORANGING: Autoranges up at 105% of range, down at 10% of range.

OHMS (cont'd)

2-WIRE RESISTANCE READING RATES[10,12] 20Ω, 200Ω, 2kΩ, and 20kΩ Ranges

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS/SECOND TO MEMORY Auto Zero Off	READINGS/SECOND TO MEMORY Auto Zero On	READINGS/SECOND TO IEEE-488 Auto Zero Off	READINGS/SECOND TO IEEE-488 Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero On
10	167 ms (200 ms)	28	7½	6 (5.1)	2 (1.7)	5 (4)	2 (1.6)	5 (4)	2 (1.6)
2	33.4 ms (40 ms)	26	7½	30 (25)	8 (7.1)	28 (23)	8 (6.8)	27 (22)	8 (6.7)
1	16.7 ms (20 ms)	25	6½	58 (48)	40 (34)	53 (45)	37 (32)	49 (41)	35 (31)
0.2[11]	3.34 ms (4 ms)	22	6½	219 (189)	109 (97)	197 (162)	97 (87)	140 (129)	79 (74)
0.1[11]	1.67 ms (2 ms)	21	5½	300 (300)	126 (118)	248 (245)	112 (108)	164 (163)	89 (88)
0.02[11]	334 µs (400 µs)	19	5½	300 (300)	130 (130)	249 (249)	114 (114)	165 (165)	91 (91)
0.01[11]	167 µs (167 µs)	16	4½	421 (421)	135 (135)	306 (306)	114 (114)	189 (189)	92 (92)
0.01[8,11]	167 µs (167 µs)	16	4½	2000 (2000)		2000(2000)			

2-WIRE RESISTANCE READING RATES[10,12] 20MΩ Range

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS/SECOND TO MEMORY Auto Zero Off	READINGS/SECOND TO MEMORY Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero On
10	167 ms (200 ms)	28	7½	6 (5.1)	1 (0.8)	2 (1.8)	1 (0.8)
2	33.4 ms (40 ms)	26	7½	30 (25)	1 (0.8)	16(14.5)	1 (0.8)
1	16.7 ms (20 ms)	25	6½	58 (48)	4 (3.8)	25 (22)	4 (3.5)
0.1[11]	1.67 ms (2 ms)	21	5½	300 (296)	5 (5)	43 (39)	5 (4.7)
0.02[11]	334 µs (400 µs)	19	5½	300 (300)	5 (5)	43 (43)	5 (5)
0.01[11]	167 µs (167 µs)	16	4½	412 (412)	5 (5)	43 (43)	5 (5)

4-WIRE RESISTANCE READING RATES[10,12] Any Range

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS or READINGS WITH TIME STAMP/SECOND TO MEMORY or IEEE-488, AUTO ZERO ON Offset Comp. Off	Offset Comp. On
10	167 ms (200 ms)	28	7½	2 (1.6)	0.6 (0.5)
2	33.4 ms (40 ms)	26	7½	7 (6.1)	2 (1.6)
1	16.7 ms (20 ms)	25	6½	12 (11.6)	3 (3.7)
0.1[11]	1.67 ms (2 ms)	21	5½	20 (20)	6 (6)
0.01[11]	167 µs (167 µs)	16	4½	21 (21)	7 (7)

OHMS NOTES

1. Current source is typically ±9% absolute accuracy.
2. Total of measured value and lead resistance cannot exceed full scale.
3. Maximum offset compensation plus source current times measured resistance must be less than source current times resistance range selected.
4. For 2-wire mode.
5. Specifications are for 1 power line cycle, 10 reading digital filter, Auto Zero on, 4-wire mode, offset compensation on (for 20Ω to 20kΩ ranges).
6. For T_{CAL} ±1°C, following 55 minute warm-up. T_{CAL} is ambient temperature at calibration (23°C at the factory).
7. For T_{CAL} ±5°C, following 55-minute warm-up. Specifications include traceability to US NIST.
8. In burst mode, display off. Burst mode requires Auto Zero refresh (by changing resolution or measurement function) once every 24 hours.
9. For T_{CAL} ±5°C, 90-day accuracy. 1-year and 2-year accuracy can be found by applying the same speed accuracy ppm changes to the 1-year or 2-year base accuracy.
10. For DELAY=0, digital filter off, internal trigger, display off. Aperture is reciprocal of line frequency. These rates are for 60Hz and (50Hz). Speed for 200kΩ range is typically 10% slower than 20kΩ range; speed for 2MΩ range is typically 3 times faster than 20MΩ range; speed for 1GΩ range is typically 30%–50% as fast as 20MΩ range. See Operating Speed section for additional detail.
11. Ohms measurements at rates lower than 1 power line cycle are subject to potential noise pickup. Care must be taken to provide adequate shielding.
12. Typical values.
13. When measuring resistance of inductive loads, the inductance of that load must be 10mH or less.

DC AMPS

DCI INPUT CHARACTERISTICS AND ACCURACY[4]

RANGE	FULL SCALE	RESOLUTION	DEFAULT RESOLUTION	MAXIMUM BURDEN VOLTAGE[6]	ACCURACY[1] ±(ppm of reading + ppm of range) 24 Hours[2]	90 Days[3]	1 Year[3]	2 Years[3]	TEMPERATURE COEFFICIENT ±(ppm of reading + ppm of range)/°C Outside T_{CAL} ±5°C
200 µA	210.00000	10 pA	100 pA	0.25 V	63 + 25	300 + 25	500 + 25	1350 + 25	58 + 7
2 mA	2.1000000	100 pA	1 nA	0.31 V	64 + 20	300 + 20	400 + 20	750 + 20	58 + 5
20 mA	21.000000	1 nA	10 nA	0.4 V	65 + 20	300 + 20	400 + 20	750 + 20	58 + 5
200 mA	210.00000	10 nA	100 nA	0.5 V	96 + 20	300 + 20	500 + 20	750 + 20	58 + 5
2 A	2.1000000	100 nA	1 µA	1.5 V	500 + 20	600 + 20	900 + 20	1350 + 20	58 + 5

DC CURRENT UNCERTAINTY = ±[(ppm reading)×(measured value) + (ppm of range)×(range used)] / 1,000,000.

% ACCURACY = (ppm accuracy) / 10,000.

10PPM OF RANGE = 20 counts at 6½ digits.

DCI READING RATES[5,9]

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS/SECOND TO MEMORY Auto Zero Off	READINGS/SECOND TO MEMORY Auto Zero On	READINGS/SECOND TO IEEE-488 Auto Zero Off	READINGS/SECOND TO IEEE-488 Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero On
10	167 ms (200 ms)	28	7½	6 (5.1)	2 (1.7)	6 (4.8)	2 (1.6)	6 (4.8)	2 (1.6)
2	33.4 ms (40 ms)	26	7½	30 (24)	10 (8.2)	28 (23)	9 (7.8)	27 (22)	9 (7.7)
1	16.7 ms (20 ms)	25	6½	57 (48)	45 (38)	53 (45)	41 (35)	48 (41)	40 (32)
0.2	3.34 ms (4 ms)	22	6½	217 (195)	122 (111)	186 (168)	109 (98)	135 (125)	88 (85)
0.1	1.67 ms (2 ms)	21	5½	279 (279)	144 (144)	234 (229)	123 (123)	158 (156)	99 (98)
0.02	334 µs (400 µs)	19	5½	279 (279)	148 (148)	234 (234)	130 (130)	158 (158)	101 (101)
0.01	167 µs (167 µs)	16	4½	298 (298)	150 (150)	245 (245)	132 (132)	164 (164)	102 (102)
0.01[7]	167 µs (167 µs)	16	4½	2000 (2000)		2000 (2000)			

DC AMPS (cont'd)

SPEED AND ACCURACY[8] 90 Days

RANGE	ACCURACY ± (ppm of reading + ppm of range + ppm of range rms noise[9]) 1 PLC DFILT Off	0.1 PLC DFILT Off	0.01 PLC[7] DFILT Off
200 µA	300+25+0.3	300+50+8	300+200+80
2 mA	300+20+0.3	300+45+8	300+200+80
20 mA	300+20+0.3	300+45+8	300+200+80
200 mA	300+20+0.3	300+45+8	300+200+80
2 A	600+20+0.3	600+45+8	600+200+80

PLC = Power Line Cycle. DFILT = Digital Filter.

SETTLING CHARACTERISTICS: <500µs to 50ppm of step size. Reading settling times are affected by source impedance and cable dielectric absorption characteristics. Add 50ppm of range for first reading after range change.

MAXIMUM ALLOWABLE INPUT: 2.1A, 250V.

OVERLOAD PROTECTION: 2A fuse (250V), accessible from front (for front input) and rear (for rear input).

AUTORANGING: Autoranges up at 105% of range, down at 10% of range.

DC AMPS NOTES

1. Specifications are for 1 power line cycle, Auto Zero on, 10 reading digital filter.
2. For T_{CAL} ± 1°C, following 55 minute warm-up.
3. For T_{CAL} ± 5°C, following 55 minute warm-up. Specifications include traceability to US NIST.
4. Add 50 ppm of range for current above 0.5A for self heating.
5. For DELAY=0, digital filter off, display off. Internal trigger. Aperture is reciprocal of line frequency. These rates are for 60Hz and (50Hz). See Operating Speed section for additional detail.
6. Actual maximum voltage burden = (maximum voltage burden) × ($I_{MEASURED}/I_{FULL\ SCALE}$).
7. In burst mode, display off. Burst mode requires Auto Zero refresh (by changing resolution or measurement function) once every 24 hours.
8. For T_{CAL} ±5°C, 90-day accuracy. 1-year and 2-year accuracy can be found by applying the same speed accuracy ppm changes to the 1-year or 2-year base accuracy.
9. Typical values.

DC IN-CIRCUIT CURRENT

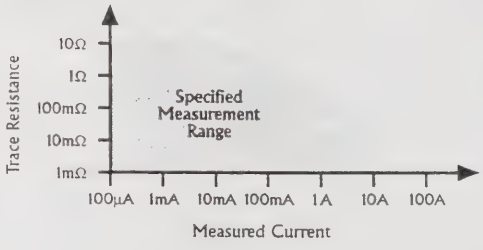
The DC in-circuit current measurement function allows a user to measure the current through a wire or a circuit board trace without breaking the circuit.

When the In-Circuit Current Measurement function is selected, the 2001 will first perform a 4-wire resistance measurement, then a voltage measurement, and will display the calculated current.

TYPICAL RANGES:

Current:	100µA to 12A.
Trace Resistance:	1mΩ to 10Ω typical.
Voltage:	±200mV max. across trace.
Speed:	4 measurements/second at 1 power line cycle.
Accuracy:	±(5% + 2 counts). For 1 power line cycle, Auto Zero on, 10 reading digital filter, T_{CAL} ±5°C, after being properly zeroed. 90 days, 1 year or 2 years.

MEASUREMENT RANGE CHART



AC AMPS

AC magnitude: RMS or Average.

ACI INPUT CHARACTERISTICS

RMS RANGE	PEAK INPUT	FULL SCALE RMS	RESOLUTION	DEFAULT RESOLUTION	MAXIMUM BURDEN VOLTAGE[5]	TEMPERATURE COEFFICIENT ± (% of reading + % of range)/°C Outside T_{CAL} ± 5°C
200 µA	1 mA	210.0000	100 pA	1 nA	0.25 V	0.01 + 0.001
2 mA	10 mA	2.100000	1 nA	10 nA	0.31 V	0.01 + 0.001
20 mA	100 mA	21.00000	10 nA	100 nA	0.4 V	0.01 + 0.001
200 mA	1 A	210.0000	100 nA	1 µA	0.5 V	0.01 + 0.001
2 A	2 A	2.100000	1 µA	10 µA	1.5 V	0.01 + 0.001

ACI ACCURACY[1,2] 90 Days, 1 Year or 2 Years, T_{CAL} ± 5°C, for 5% to 100% of range, ± (% of reading + % of range)

RANGE	20Hz–50Hz	50Hz–200Hz	200Hz–1kHz	1kHz–10kHz	10kHz–30kHz[3]	30kHz–50kHz[3]	50kHz–100kHz[3]
200 µA	0.35 + 0.015	0.2 + 0.015	0.4 + 0.015	0.5 + 0.015			
2 mA	0.3 + 0.015	0.15 + 0.015	0.12 + 0.015	0.12 + 0.015	0.25 + 0.015	0.3 + 0.015	0.5 + 0.015
20 mA	0.3 + 0.015	0.15 + 0.015	0.12 + 0.015	0.12 + 0.015	0.25 + 0.015	0.3 + 0.015	0.5 + 0.015
200 mA	0.3 + 0.015	0.15 + 0.015	0.12 + 0.015	0.15 + 0.015	0.5 + 0.015	1 + 0.015	3 + 0.015
2 A	0.35 + 0.015	0.2 + 0.015	0.3 + 0.015	0.45 + 0.015	1.5 + 0.015	4 + 0.015	

AC CURRENT UNCERTAINTY = ±[(% of reading) × (measured value) + (% of range) × (range used)] / 100.

PPM ACCURACY = (% accuracy) × 10,000.

0.015% OF RANGE = 30 counts at 5½ digits.

AC COUPLING: For AC only coupling, add the following % of reading:

	20–50Hz	50–100Hz	100–200Hz
rms, Average	0.55	0.09	0.015

AC+DC COUPLING: For DC>20% of AC rms voltage, apply the following additional uncertainty, multiplied by the ratio (DC/AC rms).

	% of Reading	% of Range
rms, Average	0.05	0.1

AC AMPS (cont'd)

ACI READING RATES[3,4]

NPLC	MEASUREMENT APERTURE	BITS	DEFAULT DIGITS	READINGS/SECOND TO MEMORY Auto Zero Off	READINGS/SECOND TO MEMORY Auto Zero On	READINGS/SECOND TO IEEE-488 Auto Zero Off	READINGS/SECOND TO IEEE-488 Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero On
10	167 ms (200 ms)	28	6½	6 (5.1)	2 (1.7)	6 (4.9)	2 (1.6)	6 (4.8)	2 (1.6)
2	33.4 ms (40 ms)	26	5½	30 (25)	9 (7.9)	28 (23)	9 (7.6)	27 (22)	9 (7.5)
1	16.7 ms (20 ms)	25	5½	57 (48)	39 (35)	53 (45)	37 (33)	49 (41)	34 (30)
0.1	1.67 ms (2 ms)	21	5½	157 (136)	70 (70)	123 (123)	62 (62)	107 (107)	56 (53)
0.01	167 µs (167 µs)	16	4½	156 (136)	70 (70)	140 (140)	63 (63)	113 (113)	56 (56)
0.01[6]	167 µs (167 µs)	16	4½	2000 (2000)		2000 (2000)			

SETTLING CHARACTERISTICS: <300ms to 1% of step change
<450ms to 0.1% of step change
<500ms to 0.01% of step change

AUTORANGING: Autoranges up at 105% of range, down at 10% of range.

HIGH CREST FACTOR ADDITIONAL ERROR ± (% of reading)

Applies to rms measurements.

CREST FACTOR	1 – 2	2 – 3	3 – 4	4 – 5
ADDITIONAL ERROR	0	0.1	0.2	0.4

AVERAGE ACI MEASUREMENT

Rms specifications apply for 10% to 100% of range.

AC AMPS NOTES

1. Specifications apply for sinewave input, AC+DC coupling, 1 power line cycle, digital filter off, following 55 minute warm-up.
2. Add 0.005% of range uncertainty for current above 0.5A rms for self-heating.
3. Typical values.
4. For DELAY=0, digital filter off, display off, internal trigger. Aperture is reciprocal of line frequency. These rates are for 60Hz and (50Hz).
5. Actual maximum voltage burden = (maximum voltage burden) × (IMEASURED/IFULL SCALE).
6. In burst mode, display off. Burst mode requires Auto Zero refresh (by changing resolution or measurement function) once every 24 hours.

FREQUENCY COUNTER

FREQUENCY/PERIOD INPUT CHARACTERISTICS AND ACCURACY 90 Days, 1 Year, or 2 Years

	FREQUENCY RANGE[1]	PERIOD RANGE	DEFAULT RESOLUTION	MINIMUM SIGNAL LEVEL 1Hz–1MHz	1–5MHz	5–15MHz	MAXIMUM INPUT	TRIGGER LEVEL	ACCURACY ± (% of reading)
AC Voltage Input	1Hz–15 MHz	67 ns – 1 s	5 digits	60 mV	60 mV	350 mV	1100 V pk[1]	0–600V	0.03
AC Current Input	1Hz– 1 MHz	1 µs – 1 s	5 digits	150 µA			1 A pk	0–600mA	0.03

MEASUREMENT TECHNIQUE: Unique pulse count/time count at overflow.

TIME BASE: 7.68MHz ± 0.01%, 0°C to 55°C.

READING TIME: 420ms maximum.

TRIGGER LEVEL ADJUSTMENT: Trigger level is adjustable in 0.5% of range steps to ±60% of range in real-time using the up and down range buttons.

FREQUENCY RANGING: Autoranging from Hz to MHz.

FREQUENCY COUPLING: AC + DC or AC only.

FREQUENCY NOTES

1. Subject to 2×10^7V•Hz product (for inputs above 20V).

TEMPERATURE (RTD)

RANGE	RESOLUTION	4-WIRE ACCURACY[3] 1 Hour[2]	90 Days	1 Year	2 Years
–100° to +100°C	0.001°C	±0.005°C	±0.05°C	±0.08°C	±0.12°C
–200° to +630°C	0.001°C	±0.005°C	±0.12°C	±0.14°C	±0.18°C
–212° to +180°F	0.001°F	±0.009°F	±0.09°F	±0.15°F	±0.22°F
–360° to +1102°F	0.001°F	±0.009°F	±0.15°F	±0.18°F	±0.33°F

RTD TYPE: 100Ω platinum; DIN 43 760 or IPTS-68, alpha 0.00385, 0.00390, 0.003916, or 0.00392, 4-wire.

MAXIMUM LEAD RESISTANCE (each lead): 12Ω (to achieve rated accuracy).

SENSOR CURRENT: 1mA (pulsed).

COMMON MODE REJECTION: <0.005°C/V at DC, 50Hz, 60Hz and 400Hz, (100Ω imbalance, LO driven).

TEMPERATURE COEFFICIENT: ±(0.0013% + 0.005°C)/°C or ±(0.0013% + 0.01°F)/°C outside TCAL ±5°C.

RTD TEMPERATURE READING RATES[1] (2- or 4-Wire)

NPLC	READINGS or READINGS WITH TIME STAMP/SECOND TO MEMORY or IEEE-488 Auto Zero Off	Auto Zero On
10	1 (1)	1 (1)
2	5 (4.3)	4 (3.6)
1	7 (6.5)	6 (5.5)
0.1	12 (10.8)	9 (9)
0.01	12 (12)	10 (10)

TEMPERATURE (Thermocouple)

THERMOCOUPLE TYPE	RANGE	DEFAULT RESOLUTION	ACCURACY[4]
J	–200° to + 760°C	0.1°C	±0.5°C
K	–200° to +1372°C	0.1°C	±0.5°C
T	–200° to + 400°C	0.1°C	±0.5°C
E	–200° to +1000°C	0.1°C	±0.6°C
R	0° to +1768°C	1 °C	±3 °C
S	0° to +1768°C	1 °C	±3 °C
B	+350° to +1820°C	1 °C	±5 °C

TC TEMPERATURE READING RATES[1]

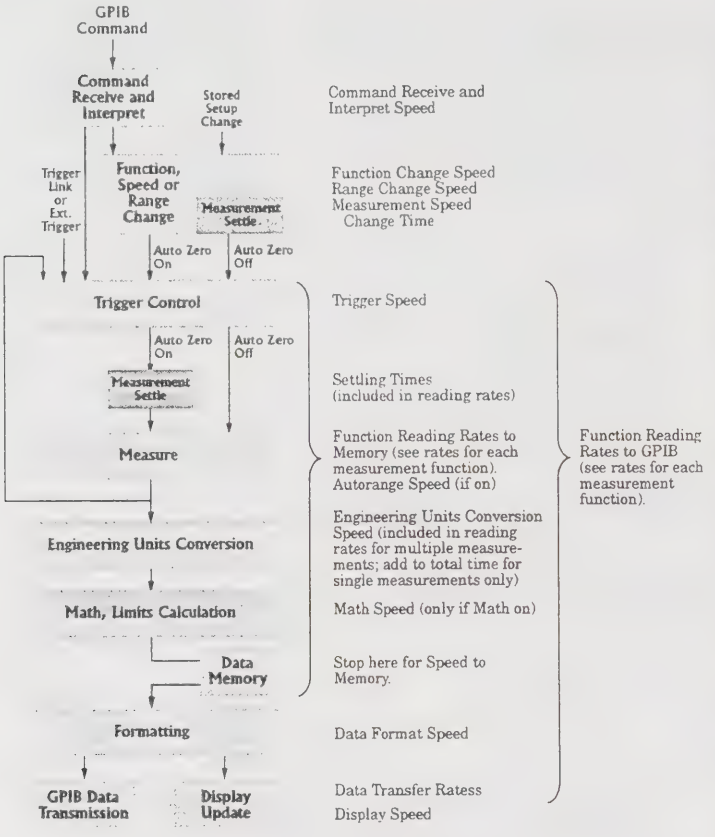
NPLC	READINGS/SECOND TO MEMORY Auto Zero Off	Auto Zero On	READINGS/SECOND TO IEEE-488 Auto Zero Off	Auto Zero On	READINGS/SECOND WITH TIME STAMP TO IEEE-488 Auto Zero Off	Auto Zero On
10	6 (5.1)	2 (1.7)	4 (3.4)	2 (1.4)	4 (3.4)	2 (1.4)
2	30 (25)	9 (7.6)	28 (23)	9 (7.3)	27 (22)	8 (7.2)
1	57 (48)	43 (37)	53 (45)	40 (32)	49 (41)	37 (30)
0.1	139 (139)	95 (95)	126 (123)	85 (84)	99 (99)	72 (72)
0.01	177 (177)	98 (98)	156 (156)	87 (87)	119 (119)	73 (73)

TEMPERATURE NOTES

1. Typical speeds for Auto Zero on. For DELAY=0, digital filter off, display off, internal trigger. Rates are for 60Hz and (50Hz).
2. For ambient temperature ±1°C, measured temperature ±10°C, 10-reading digital filter.
3. Excluding probe errors. TCAL ±5°C.
4. Relative to external 0°C reference junction; exclusive of thermocouple errors. Junction temperature may be external. Applies for 90 days, 1 year or 2 years, TCAL ±5°C.

OPERATING SPEED

The following diagram illustrates the factors that determine a DMM's reading rate.



COMMAND RECEIVE AND INTERPRET SPEED

	FASTEST	TYPICAL	SLOWEST
Time per character	0.16 ms	0.28 ms	0.66 ms
Characters per second	6250	3751	1515

TYPICAL COMMAND TIMES Command	Receive and Interpret Time	Rate (per second)
SENSE1:VOLTAGE:AC: RESOLUTION MAXIMUM	9.4 ms	106
VOLT:AC:RES:MAX	4.1 ms	243
SENSE1:FUNC 'VOLT:AC"	6.3 ms	158
RESISTANCE:RANGE:UPPER 1E9	9.0 ms	111
STATUS:QUEUE:CLEAR	5.1 ms	196
STAT:QUE:CLE	3.1 ms	322
*TRG	1.2 ms	833

MEASUREMENT SPEED CHANGE TIMES[1,2]

Typical delay before first reading after making a speed change.

FUNCTION	From	To	AUTO ZERO OFF Time	AUTO ZERO ON Time
DCV, DCI, ACI	Any	≤ 0.1 PLC	66 ms	44 ms
	Any	1 PLC	190 ms	140 ms
	Any	10 PLC	1540 ms	1195 ms
ACV	Any	≤ 0.1 PLC	120 ms	100 ms
	Any	1 PLC	250 ms	197 ms
	Any	10 PLC	1600 ms	1250 ms
Ohms (2-wire)	Any	≤ 0.1 PLC	69 ms	57 ms
	Any	1 PLC	195 ms	170 ms
	Any	10 PLC	1540 ms	1370 ms
Ohms (4-wire)	Any	≤ 0.1 PLC	110 ms	46 ms
	Any	1 PLC	240 ms	165 ms
	Any	10 PLC	1590 ms	1370 ms
TC Temperature	Any	≤ 0.1 PLC	80 ms	55 ms
	Any	1 PLC	195 ms	170 ms
	Any	10 PLC	1545 ms	1370 ms

FUNCTION CHANGE SPEED[1]

FROM Function	TO Function	Range(s)	AUTO ZERO OFF TIME	AUTO ZERO OFF RATE (per second)	AUTO ZERO ON TIME	AUTO ZERO ON RATE (per second)
Any	DCV	200mV, 2V	8.1 ms	120	36 ms	27
		20V	8.1 ms	120	8.6 ms	110
		200V	24 ms	40	52 ms	19
		1000V	11 ms	160	10.2 ms	190
Any	ACV	Any	563 ms	1.8	563 ms	1.8
Any except ACI	DCI	200µA, 2mA, 20mA	4.5 ms	220	5.1 ms	190
		200mA, 2A	6.0 ms	160	6.6 ms	150
ACI		Any	21.1 ms	45	22 ms	45
Any	ACI	Any	521 ms	1.9	521 ms	1.9
Any	Ohms (2-wire)	20Ω, 200Ω, 2kΩ, 20kΩ	6.0 ms	165	34 ms	29
		200kΩ	26 ms	38	61 ms	16
		2MΩ	95 ms	10.5	425 ms	2.4
		20MΩ	265 ms	4	690 ms	1.4
		200MΩ, 1GΩ	366 ms	3	5.5 ms	180
Any	Ohms (4-wire)	20Ω, 200Ω, 2kΩ, 20kΩ	12 ms	140	34.1 ms	29
		200kΩ	26 ms	38	60 ms	16
Any except ACI and Ohms	Frequency[8]	Any	61 ms	16	60 ms	17
ACI, Ohms (4-wire)		Any	79 ms	12	75 ms	13
Ohms (2-wire)		Any	418 ms	2	416 ms	2
Any	RTD Temp. (2-wire)	Any	6.0 ms	165	33 ms	30
	RTD Temp. (4-wire)	Any	11.5 ms	150	37 ms	27
	TC Temp.	Any	8.0 ms	125	35 ms	28

OPERATING SPEED (cont'd)

RANGE CHANGE SPEED[1]

FUNCTION	From	To	AUTO ZERO OFF TIME	AUTO ZERO OFF RATE (per second)	AUTO ZERO ON TIME	AUTO ZERO ON RATE (per second)
DCV	200mV, 2V	20V	4.5 ms	220	3.1 ms	190
	200V, 1000V	20V	8.0 ms	120	8.6 ms	110
	200mV, 2V, 20V	200mV, 2V, 20V	4.5 ms	220	36 ms	27
	200V, 1000V	200mV, 2V	8.0 ms	120	38 ms	26
	200mV, 2V, 20V	200V	24 ms	41	52 ms	19
	1000V	200V	9 ms	110	37 ms	27
	Any	1000V	11 ms	165	10.1 ms	190
ACV	Any	Any	563 ms	1.8	563 ms	1.8
DCI	Any	200µA, 2mA, 20mA	4.5 ms	220	5.2 ms	190
		200mA, 2A	6.0 ms	160	6.6 ms	150
ACI	Any	Any	525 ms	1.9	525 ms	1.9
Ohms (2-wire)	Any	20Ω, 200Ω, 2kΩ, 20kΩ	6.0 ms	160	34 ms	29
	Any	200kΩ	26 ms	38	66 ms	15
	Any	2MΩ	95 ms	10	420 ms	2.3
	Any	20MΩ	265 ms	3.7	690 ms	1.4
	Any	200MΩ, 1GΩ	366 ms	2.7	5.5 ms	180
Ohms (4-wire)	Any	20Ω, 200Ω, 2kΩ, 20kΩ	8 ms	160	34 ms	29
	Any	200kΩ	26 ms	38	66 ms	16

TRIGGER SPEED (External Trigger or Trigger-Link)

	Auto Zero On	Auto Zero Off
Trigger Latency:	1.2 ms typical	2 µs
Trigger Jitter:		±0.5 µs

ENGINEERING UNIT CONVERSION SPEED

Included in reading times for multiple measurements; add to total time for single measurements only.

CONFIGURATION	TIME	RATE (per second)
DCV	2.4 ms	416
DCV, Filter on	2.4 ms	416
DCV, Relative on	2.5 ms	400
DCV, Ratio on	3.7 ms	270
ACV	5.3 ms	188
ACV, Relative on	5.3 ms	188
ACV, Filter on	6.8 ms	147
ACV, dB	9.4 ms	106
ACV, dBm	17.3 ms	57

DISPLAY SPEED

Display updated at up to 20 times per second. Display update can be suspended by holding the display (press ENTER) or setting Display Enable Off from GPIB.

MATH AND LIMITS CALCULATION SPEED[1]

CALCULATION	NOMINAL TIME	NOMINAL RATE (per second)	MAXIMUM TIME
mX + b	0.35 ms	2850	0.44 ms
Percent	0.60 ms	1660	0.64 ms
Limits[6]	0.35 ms	2850	0.37 ms
None	0.07 ms		0.08 ms

GPIB DATA FORMATTING TRANSMISSION TIME[3]

FORMAT	READINGS ONLY Time	READINGS ONLY Rdg./s	READINGS WITH TIME STAMP Time	READINGS WITH TIME STAMP Rdg./s
DREAL (Double precision real)	0.30 ms	3330	2.0 ms	500
SREAL (Single precision real)	0.37 ms	2710	2.1 ms	475
ASCII	3.9 ms	255	8.2 ms	120

SINGLE FUNCTION SCAN SPEED[4] (Internal Scanner)

TYPE	DCV (20V)[7] Time per Chan.	DCV (20V)[7] Rate (Chan./second)	2-Wire Ohms (2kΩ)[7] Time per Chan.	2-Wire Ohms (2kΩ)[7] Rate (Chan./second)	4-Wire Ohms (2kΩ)[7] Time per Chan.	4-Wire Ohms (2kΩ)[7] Rate (Chan./second)	ACV Time per Chan.	ACV Rate (Chan./second)	Frequency Time per Chan.	Frequency Rate (Chan./second)	TC Temperature Time per Chan.	TC Temperature Rate (Chan./second)	RTD Temperature (2-Wire) Time per Chan.	RTD Temperature (2-Wire) Rate (Chan./second)
Ratio or Delta[5] (2 channels)	4 ms	250	4.4 ms	230	18.5 ms	54								
Fast Scan (using solid state channels)	5.5 ms	181	7 ms	140			520 ms	1.9	958 ms	1	13.8 ms	72		
Normal Scan	10.3 ms	97	12.1 ms	80	21 ms	47	532 ms	1.8	974 ms	1	18 ms	55	95 ms	10

MIXED FUNCTION SCAN SPEED[1] (Internal Scanner)

SCAN CONFIGURATION (Channels)	Average Time/ Channel	Average Rate (Channel/s)
5 chan. DCV, 5 chan. 2wΩ	20 ms	50
3 DCV, 3 2wΩ, 4 TC	22 ms	45
5 2wRTD, 5 TC	60 ms	17
5 2wΩ, 5 2wRTD	60 ms	17
9 DCV, 1 ACV	73 ms	13
2 DCV, 1 ACV, 2 2wΩ, 1 4wΩ	122 ms	8
5 DCV, 5 Freq.	490 ms	2
3 DCV, 3 ACV, 2 4wΩ	220 ms	5

OPERATING SPEED NOTES

1. With Display off, 1 power line cycle, autorange off, filter off, triggers halted. Display on may impact time by 3% worst case. To eliminate this impact press ENTER (hold) to lock out display from front panel.
2. Based on using 20V, 2kΩ, 200mA ranges.
3. Auto Zero off, using 386SX/16 computer, average time for 1000 readings, byte order swapped, front panel disabled.
4. Typical times for 0.01 power line cycle, autorange off, Delay=0, 100 measurements into buffer.
5. Ratio and delta functions output one value for each pair of measurements.
6. Time to measure, evaluate limits, and set digital outputs are found by summing measurement time with limits calculation time.
7. Auto Zero off.
8. Based on 100kHz input frequency.

DELAY AND TIMER

TIME STAMP

Resolution: 1µs.
Accuracy: ±0.01% ±1µs.
Maximum: 2,100,000.000 000 seconds (24 days, 20 hours).

DELAY TIME (Trigger edge to reading initiation)

Maximum: 999,999.999 seconds (11 days, 12 hours).
Resolution: 1ms.
Jitter: ±1ms.

TIMER (Reading initiation to reading initiation)

Maximum: 999,999.999 seconds (11 days, 12 hours).
Resolution: 1ms.
Jitter: ±1ms.

NOTE: To find measurement speed, see each measurement section.

MAXIMUM INPUT LEVELS

	RATED INPUT[1]			OVERLOAD RECOVERY TIME
HI to LO	±1100V pk			< 900 ms
HI Sense to LO	± 350V pk	250V rms		< 900 ms
LO Sense to LO	± 350V pk	250V rms		< 900 ms
I Input to LO	2A, ± 250V		(fused)	—
HI to Earth	±1600V			< 900 ms
LO to Earth	± 500V			

1. For voltages between other terminals, these ratings can be algebraically added.

IEEE-488 BUS IMPLEMENTATION

IMPLEMENTATION: IEEE-488.2, SCPI-1991.0.
MULTILINE COMMANDS: DCL, LLO, SDC, GET, GTL, UNT, UNL, SPE, SPD.
UNILINE COMMANDS: IFC, REN, EOI, SRQ, ATN.
INTERFACE COMMANDS: SH1, AH1, T5, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, C0, E1.

DIGITAL I/O

CONNECTOR TYPE: 8 pin "D" subminiature.
INPUT: One pin, TTL compatible.
OUTPUTS: Four pins. Open collector, 30V maximum pull-up voltage, 100mA maximum sink current, 10Ω output impedance.
CONTROL: Direct control by output or set real-time with limits.

GENERAL SPECIFICATIONS AND STANDARDS COMPLIANC

POWER

Voltage: 90–134V and 180–250V, universal self-selecting.
Frequency: 50Hz, 60Hz, or 400Hz self-identifying.
Consumption: <55VA.

ENVIRONMENTAL

Operating Temperature: 0°C to 50 °C.
Storage Temperature: –40 °C to 70 °C.
Humidity: 80% R.H., 0°C to 35°C, per MIL-T-28800E[1] Para 4.5.5.1.2.

NORMAL CALIBRATION

Type: Software. No manual adjustments required.
Sources: 2 DC voltages (2V, 20V) and 2 resistances (19k and 1M). Different calibration source values are allowed. All other functions calibrated (adjusted) from these sources and a short circuit. No AC calibrator required for adjustment.

PHYSICAL

Case Dimensions: 90mm high × 214mm wide × 369mm deep (3½ in. × 8½ in. × 14½ in.).
Working Dimensions: From front of case to rear including power cord and IEEE-488 connector: 15.0 inches.
Net Weight: <4.2kg (<9.2 lbs.).
Shipping Weight: <9.1kg (<20lbs.).

STANDARDS

EMI/RFI: Conforms to VDE 0871B (per Vfg 1046/1984), IEC 801-2. Meets FCC part 15 Class B, CISPR-22 (EN55022).
Safety: Conforms to IEC348, CAN/CSA-C22.2. No. 231, MIL-T-28800E[1]. Designed to UL1244.
Reliability: MIL-T-28800E[1].
Maintainability: MIL-T-28800E[1].
MTTR: <90 minutes (includes disassembly and assembly, excludes recalibration). MTTR is Mean Time To Repair.
MTBF, Estimated: >75,000 hours (Bellcore method). MTBF is Mean Time Between Failure.
MTTC: <20 minutes for normal calibration. <6 minutes for AC self-calibration. MTTC is Mean Time To Calibrate.
Process: MIL-STD 45662A and BS5750.

ACCESSORIES SUPPLIED

The unit is shipped with line cord, high performance modular test leads, user's manual, option slot cover, and full calibration data. A personal computer startup package is available free.

Note 1: For MIL-T-28800E, applies to Type III, Class 5, Style E.

EXTENDED MEMORY / NON-VOLATILE MEMORY OPTION

	DATA STORAGE				SETUP STORAGE	
MODEL	SIZE (Bytes)	4½-Digit	6½-Digit w/Time Stamp	Type	Number	Type
2001	8k	2,027	404	volatile	1	non-volatile
2001/MEM1	32k	6,909	1,381	non-volatile	5	non-volatile
2001/MEM2	128k	29,908	5,980	non-volatile	10	non-volatile

These are the minimum sizes to expect.

Specifications subject to change without notice.

KEITHLEY

Service Form

Model No. _____ **Serial No.** _____ **Date** _____

Name and Telephone No. _____

Company _____

List all control settings, describe problem and check boxes that apply to problem. _____

_____

_____

- ❑ Intermittent
- ❑ IEEE failure
- ❑ Front panel operational
- ❑ Analog output follows display
- ❑ Obvious problem on power-up
- ❑ All ranges or functions are bad
- ❑ Particular range or function bad; specify _____
- ❑ Batteries and fuses are OK
- ❑ Checked all cables

Display or output (check one)

- ❑ Drifts
- ❑ Unstable
- ❑ Overload
- ❑ Unable to zero
- ❑ Will not read applied input

- ❑ Calibration only
- ❑ Data required
- ❑ Certificate of calibration required

(attach any additional sheets as necessary)

Show a block diagram of your measurement system including all instruments connected (whether power is turned on or not). Also, describe signal source.

Where is the measurement being performed? (factory, controlled laboratory, out-of-doors, etc.)

_____

_____

What power line voltage is used? _____ Ambient temperature? _____ °F

Relative humidity? _____ Other? _____

Any additional information. (If special modifications have been made by the user, please describe.)

_____

_____

Be sure to include your name and phone number on this service form.